DIGITAL FREQUENCY SYNTHESIZER

The DFS produces the necessary frequencies to transmit and receive on all 23 citizen band channels from one crystal controlled REFERENCE OSCILLATOR Q9. The crystal X1 in oscillator Q9 is in series with varactor D14. In TX mode a forward bias across D14 causes Q9 to oscillate at 10.2381 MHz; in RX mode a reverse bias adjustable by DELTA TUNE control VR5 causes it to oscillate around 10.240 MHz. The output of Q9 is fed to a 10 stage binary counter formed by IC-5, -6, -7 and -8 which divides the frequency by 1024 to produce about 10 KHz in RX mode and 9.998 in TX mode. This signal is compared by a PHASE-FREQUENCY and LOSS-OF-LOCK DETECTOR IC-9 with the signal from the PROGRAMMABLE COUNTER formed by IC-1, -2, -3 and -4 which is driven by oscillator Q21. When the output of the 10 stage counter is not in phase with that of the PROGRAMMABLE COUNTER the LOSS-OF-LOCK DETECTOR outputs a signal that disables the transceiver. The FREQUENCY DETECTOR produces an error voltage which is added to the bias on varactor D26, and varies the frequency of the VCO (VOLTAGE CONTROLLED OSCILLATOR) Q21. The output of the PROGRAMMABLE COUNTER is thus brought into frequency and phase lock with the 10 stage counter. While the 10 stage counter divides by 1024 (2^{10}), the programmable counter is determined by the A, B, C, D, & E inputs from the CHANNEL SELECTOR. The A, B, C, D, & E inputs are determined by the particular channel selected. (See Table 5-15.)

PROGRAMMABLE DIVIDER

The PROGRAMMABLE DIVIDER divides the output frequency of the VCO Q21, such that when Q21 is operating at the proper frequency, the PROGRAMMABLE DIVIDER's output will be equal in frequency and phase to the output of the REFERENCE DIVIDER. While the ratio of the REFERENCE DIVIDER is fixed at 1024, the ratio of the PROGRAMMABLE DIVIDER is determined by the channel selected by the CHANNEL SELECTOR. (See Table 5-15.) Three 4-bit counters, IC-1, -2 & -3 are cascaded to form a 12-bit counter. The count outputs of IC-1 & -2 are fed to open collector NAND gates in IC-4. The outputs of these NAND gates are wire ANDed to drive the $\overline{PE}$ (Preset Enable when low) and an input of the PHASE-FREQUENCY COMPARATOR. In TX mode pin 10 of G2 is grounded. This disables it such that G1 determines the terminal count and stuffs the counter with the channel select code. Pin 10 is high in RX mode permitting G2 to determine the terminal count. Thus the channel select code sets the initial count and G1 in TX mode or G2 in RX mode determines terminal count. Counting is therefore cyclical and each cycle is accompanied by a preset pulse which is the programmed divide ratio.

CHANNEL SELECTOR

The CHANNEL SELECTOR selects the operating channel for the SBE-32CB in response to the UP and DN buttons located on the MIC HEAD. The CHANNEL SELECTOR feeds the DIGITAL FREQUENCY SYNTHESIZER and the display circuitry in the MIC HEAD.

The UP or DN button on the MIC HEAD sets FF-1 or FF-2 respectively. Setting FF-1 produces a low pulse out pin 8 of IC-11 which is differentiated by C4, R15 & R16 and then used to pulse the up count on the 8-stage binary counter IC-12 & IC-13. Likewise, setting FF-2 will pulse the DN count. If either the UP or DN button is held, C1 will charge and fire PUT CR1. The PUT will then initiate UP or DN pulses as long as the button is pressed. The output of the counter feeds two ROMs — IC-16 and IC-17. IC-17 converts the count to BCD which is then fed to the MIC HEAD display circuitry. IC-16 converts the count to the channel select code which is fed to the DIGITAL FREQUENCY SYNTHESIZER. (See Table 5-5.) IC-16 produces a low output on pin 7 when the count is 23 and a low output on pin 9 when the count is **1**. Otherwise, pin 7 and 9 are high. The output on pin 7 of IC-16 drives pin 1 on IC-18 low which then drives pin 9 on IC-15 high enabling an UP pulse to load the counter with the inputs at the preset (pins 1, 9, 10, 15). Since pin 3 of IC-15 is low a **1** is loaded. Likewise, a **1** output from the counter enables a DN pulse to load it, but since pin 3 of IC-15 is now high a 10111 or 23 is loaded.

A **1** is loaded when the unit powers up. In the off position, S4 forward biases the base of Q27 discharging C2. When S4 is turned on, Vcc pulls the anode of SCR CR2 high. C2 charges; CR2 fires and the anode goes low. This initial high anode pulse feeds pin 5 of IC-18 and is inverted out pin 6 and loads a **1** in the counter.

SYNCHRONOUS UP/DOWN PRESETTABLE 4-BIT BINARY COUNTER

The two M53200P (IC-12 & IC-13) UP/DOWN COUNTERs are used in the SBE-32CB CHANNEL SELECTOR for generating the channel number. The count up or down is triggered by a low-to-high pulse edge. By feeding the borrow of IC-12 to the DN of IC-13 and the carry of IC-12 to the UP of IC-13, these counters are cascaded to form an 8-bit binary counter. When the $\overline{LD}$ input is driven low, the preset inputs are loaded, and override the count. It is necessary for counting that pin 16 (Vcc), pin 11 ($\overline{LD}$) be high and pin 14 (clear) and pin 8 (GND) be low. When either the UP or DN (pin 4 or 5 respectively) is pulsed the other must be high. (See Table 5-17, -18.)

BINARY TO BCD CONVERTER

The M53385P (IC-17) converts the binary input from the counter to BCD. (See Table 5-21.)

PROGRAMMABLE READ ONLY MEMORY

The M547305 PROM converts the binary inputs from the counter to channel-select-codes and indicates to the counter preset logic if the counter output is 1 or 23. (See Table 5-20.)

BCD TO 7-SEGMENT DRIVER

The 7447 converts the BCD to 7-SEGMENT and drives the LED channel display in the MIC HEAD.

FIG. 4-1 TRANSCEIVER BLOCK DIAGRAM

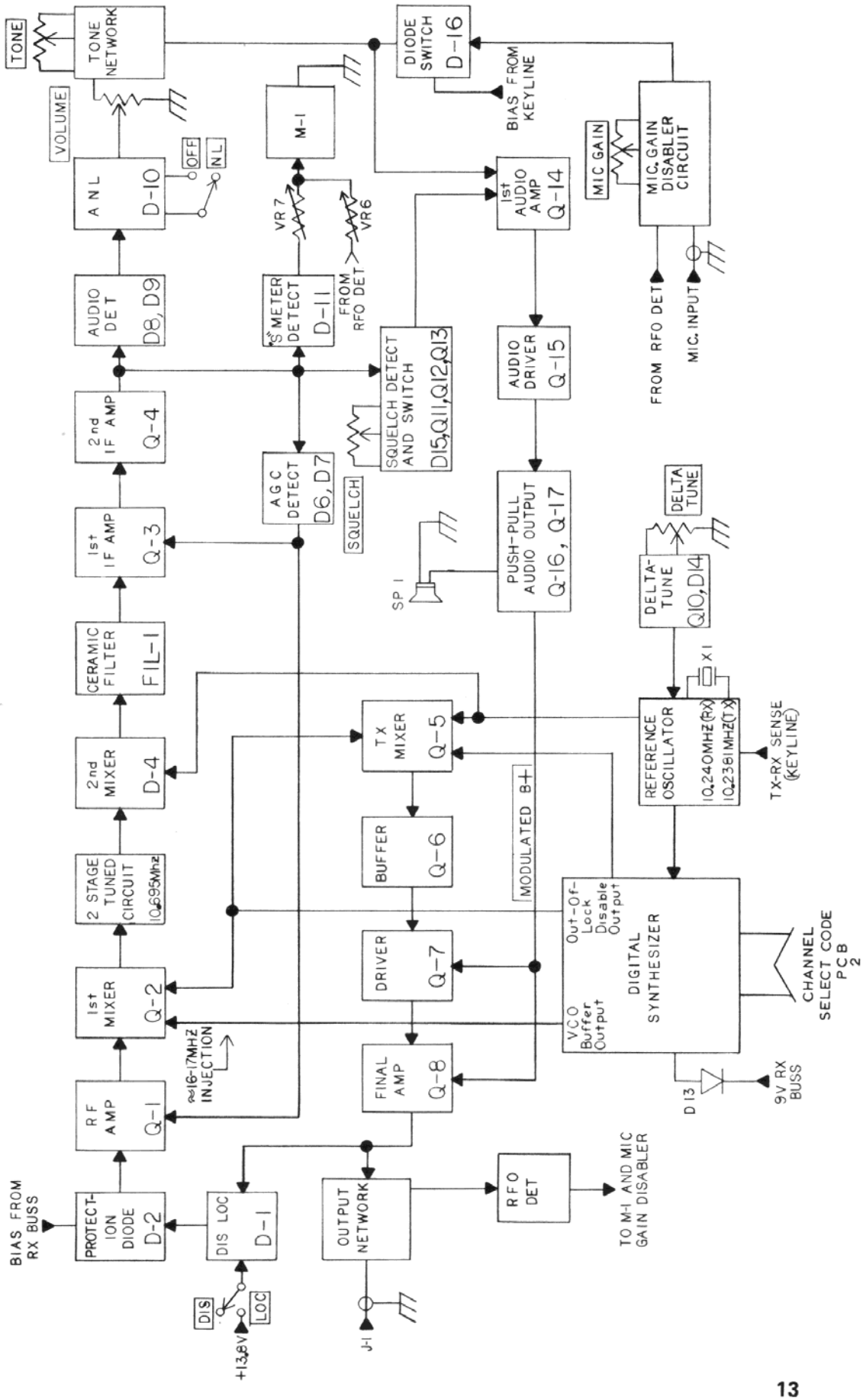


FIG. 4-2 SYNTHESIZER BLOCK DIAGRAM

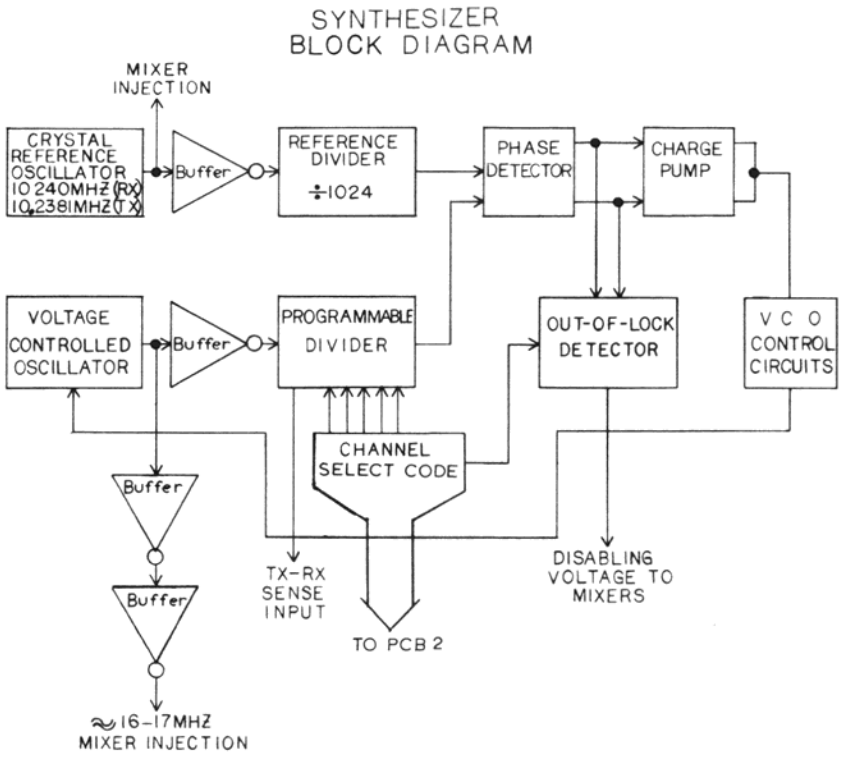
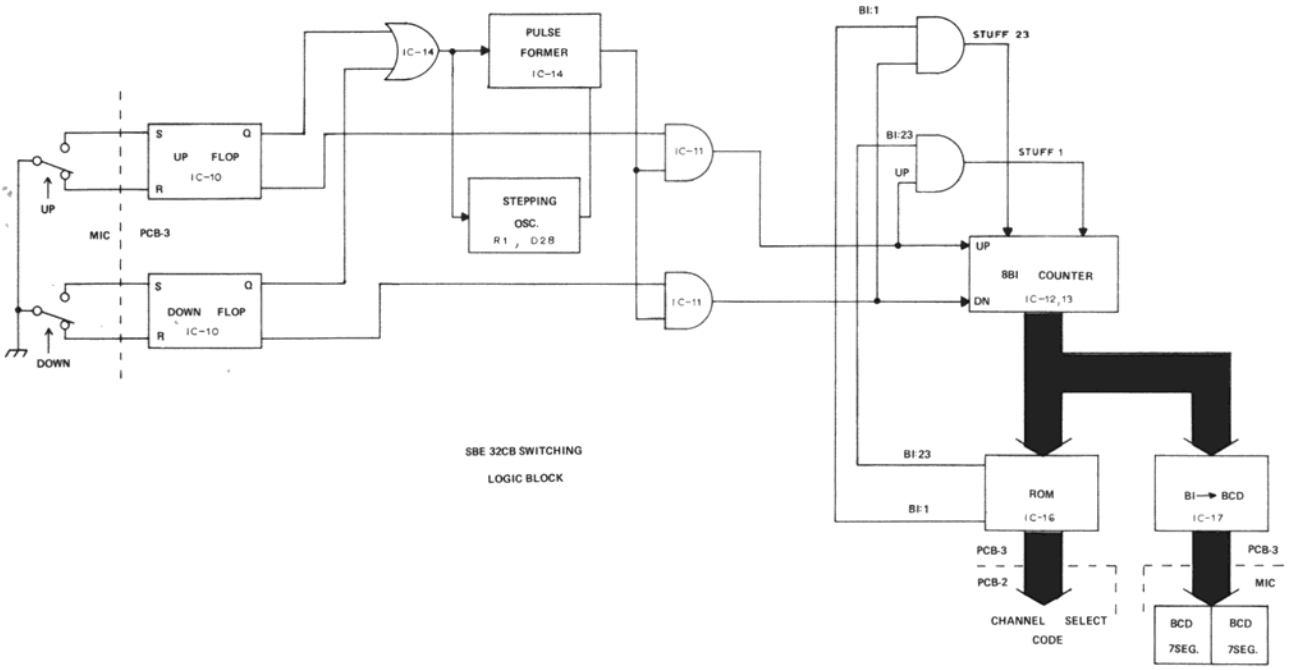


FIG. 4-3 CHANNEL SELECTOR BLOCK DIAGRAM



SECTION 5

SERVICING

5.1 INTRODUCTION

Read this section carefully before attempting any repair of the SBE-32CB. Refer to the circuit description, block and schematic diagrams. The transistor and IC case diagrams are shown on the schematic diagram. Refer to these diagrams before checking transistors or ICs. Component layout prints are provided to aid troubleshooting and alignment. **Use only recommended replacement parts.** Refer to the parts list in the back of this book. **Never replace blown fuses with higher rated ones or fast acting with slow blow.** To check operation of the unit, refer to Table 5-2, PERFORMANCE VERIFICATION PROCEDURE. Figures 5-3, 5-4, TRANSMITTER TEST CONNECTION and RECEIVER TEST CONNECTION respectively, show the proper manner to connect the unit to test instruments for performance verification or alignment. Table 5-1 lists RECOMMENDED TEST INSTRUMENTS. Tables 5-6, 5-9 show proper TRANSMITTER ALIGNMENT PROCEDURE and RECEIVER ALIGNMENT PROCEDURE respectively. Figure 5-10, ALIGNMENT LAYOUT is placed next to the alignment procedures to show alignment adjustments at a glance.

5.2 TEST SIGNALS

OSCILLOSCOPE WAVEFORMS are shown which were taken at various points in the SBE-32CB during normal operation into a dummy load. CHECK POINT numbers next to the waveform pictures correspond to numbers in boxes on both the schematic diagrams and component layout drawing. Some waveforms are shown on the schematic diagrams. The waveforms on the CHANNEL SELECTOR schematic are shown for auto scan mode. Figure 5-7 shows RF amplification through a properly aligned transmitter. Figure 5-8 shows 50%, 100% and overmodulation respectively. Notice that the waveform at the drain of Q5 – the TX MIXER – contains several frequency components. Also notice that the waveform at the collector of Q8 – the TX FINAL – is unsymmetrical (Figure 5-7C). This is proper since the TX FINAL operates class C for greater efficiency. Figure 5-7d shows how the output should look at the dummy load.

VOLTAGE MEASUREMENTS are shown on the schematic diagram for normal operation. All voltages were measured with a voltmeter having 10MΩ input impedance. Voltage measurements on high impedance RF points should be taken through a choke. While any choke about 100μH is suitable, SBE part 8000-00011-0018 (150μH) may be ordered from the factory. Mini-test clips are very useful for making voltage measurements in hard to reach places.

RECEIVER INJECTION VOLTAGES are given in Table 5-11 together with CHECK POINT numbers which correspond to numbers in boxes on both the schematic diagram and component layout drawing. This table specifies the voltage level, carrier frequency and particular points in the receiver string at which a 30% – 1 KHz modulated signal injected through a .01 MFD capacitor should produce at least 2 VAC of audio across the speaker or 8Ω load plugged into the speaker jack, EXT SP. While the value of this capacitor is not critical, capacitive coupling of the signal generator to the circuit is necessary to prevent grounding out the transistor biases.

Before setting up to measure RECEIVER INJECTION VOLTAGES, small hand-held "all purpose signal generators" can be used to provide a quick check of the receiver string. Basically, these devices generate pulses rich in harmonics from AF to RF to test whether a stage is working.

AGC VOLTAGES versus RF INPUT LEVEL are shown in Table 5-13. This table should be consulted before any adjustments are made on the squelch circuit since squelch is a function of AGC.

Table 5-12, SYNTHESIZER TROUBLESHOOTING PROCEDURE, should be used as a guide to locating problems in the FREQUENCY SYNTHESIZER.

Table 5-14, DEFECT IN CHANNEL SELECT CODE, shows which channels are affected by failure of the SYNTHESIZER to respond to a bit of the CHANNEL SELECT CODE. This may be a failure of a voltage to appear on an input pin of an IC or **it may also be a defect in the input of the particular IC.**

FREQUENCY MEASUREMENTS are shown which were taken at various points in the FREQUENCY SYNTHESIZER during normal operation and are shown on both the schematic diagram and component layout drawing. If the frequencies are wrong then ascertain where the ratios are wrong. Start by measuring the frequency of the REFERENCE or PROGRAMMABLE DIVIDER'S DRIVER Q24 or Q25 respectively. Divide the "normal" frequency by the "wrong" frequency. Using this ratio as a multiply-constant, go through the divider multiplying frequencies by this constant. A defect in a divider is indicated whenever the constant times the wrong frequency does not equal the normal frequency. This technique is greatly facilitated by a pocket calculator with memory.

LOGIC FUNCTION TABLES (5-15 through 5-21) show the logic states in the CHANNEL SELECTOR during normal operation. The high, low or pulse states are best determined with a logic probe. The Hewlett Packard HP 1052T logic probe is recommended. This probe is bright and can be seen at any angle. An oscilloscope can be used to determine high or low levels; a high should be greater than 2 volts and a low less than 0.8 volts.

Before removing an IC, try to make certain that it is the trouble. Use a low wattage soldering iron and solder wick. Make certain that all of the IC's pins are free before attempting to remove it from the board.

A blown fuse should only be replaced by one of the proper rating and type. If the fuse blows again, replace it, but place an Ω meter at the power terminals in place of the supply. Make certain that the + side of the Ω meter is connected to the red power wire of the SBE-32CB. Some VOMs place the – side of the Ω meter out the red test jack. Observe that D22 protects the unit from a reversed supply.

A fuse may blow only when the unit is connected in a vehicle because the vehicle has a positive ground and there is a short from the PCB ground to the chassis, or a grounded speaker was plugged into EXT SP J2.

The second harmonic trap (L10 and CV1) is adjusted at the Factory; field adjustment should not be attempted without proper equipment.

FIG. 5-1 RECOMMENDED TEST INSTRUMENTS

TEST INSTRUMENT	REQUIRED SPECIFICATIONS	USE	RECOMMENDED INSTRUMENT TYPE
R.F. Signal Generator	Output frequency: 26.965 to 27.255 MHz. Output level calibrated from .1 microvolts to 500,000 microvolts. Internal modulation capability of 30% minimum at 1 KHz. (Calibrated)	Receiver service and alignment.	Hewlett-Packard Model 606A or B. Wavetek Model 3000.
Oscilloscope	Vertical bandwidth of 25 MHz or greater at 3db point. Triggered sweep capability.	Transmitter and receiver test and alignment.	Tektronics Model T932. Tektronics Model 465. Hewlett-Packard Model 180. Phillips Model PM3260E.
Frequency Counter	Frequency range DC to 30 MHz. Sensitivity: 10mv R.M.S. at 30 MHz. Overall timebase accuracy ±.002%, 6 digit resolution.	Transmitter frequency check and synthesizer troubleshooting.	Heath-Schlumburger Model SM128A
Wattmeter	5 watts full scale into 50 ohm load ±5% accuracy.	Measure power output and S.W.R.	Bird Model 43 with type 5A element. (May be terminated with antenna load
AC VTVM	-40 to +20db range.	Measure audio output.	Heath Model IM-21.
Audio Oscillator	400 Hz to 4000 Hz output: Adjustable level, 0-1 volt output impedence 600 ohm.	Audio and modulator tests.	Hewlett-Packard Model 204C. Heath Model SG18A.
DC Power Supply	13.8 volt DC ±10% at 2 amperes.	Primary supply voltage for servicing.	Heath Model SP2720 (SBE Model SBE-1AC may be used if available.)
Logic Probe	TTL: High, low and pulse.	Troubleshooting logic.	Hewlett-Packard Model 10525T.

FIG. 5-2 PERFORMANCE VERIFICATION PROCEDURE

RECEIVER

STEP 1 Connect unit to 13.8 volt DC supply.
STEP 2 Set generator frequency to 27.115 MHz with 30% modulation at 1 KHz. Connect the signal generator to the antenna jack of the transceiver.
STEP 3 Set channel selector switch to channel 13, the DIS/LOC switch to distance position, CB/PA switch to CB position, noise limiter switch to NL position and delta tune to mid-position.
STEP 4 Set signal generator output at 1μV and verify 5 volts AC audio across external speaker jack using 8Ω resistive load.
STEP 5 Turn off the signal generator modulation and verify a 10db or greater reduction in audio output.
STEP 6 Increase generator output to 100μV. Check for "S" meter indication of approximately "S9".
STEP 7 Observe meter lamp and channel selector lamp to insure that both are operational.
STEP 8 Reset generator output to 1μV. Rotate delta tune control to both extremes, verify a slight decrease in audio output and "S" meter reading at both extremes, return delta tune to center position.
STEP 9 Increase signal generator output to 200μV. Rotate squelch knob fully clockwise and verify full squelch of the receiver with an input of 200μV (tight squelch may be adjusted with VR8).

(continued)

STEP 10

Decrease generator output to 1μV, adjust squelch control to the point that the receiver is just muted. Increase signal generator output by 1/2μV and verify that the squelch opens.

STEP 11

Set CB/PA switch in the PA position. Connect an external speaker or 8Ω load across PA jack and observe the audio output while speaking into the microphone.

TRANSMITTER

STEP 1

Connect the unit to 13.8 volt DC supply. Set channel selector to channel 13, CB/PA switch to CB position. Connect standard microphone to the microphone input jack. Connect wattmeter and dummy load to antenna jack. Key the transmitter and check that the transmit lamp comes on. Observe an output of 3 watts or greater on the wattmeter. Observe a nominal internal RFO meter reading of approximately 2/3 scale. (RFO may be adjusted by VR6.)

STEP 2

Whistle into microphone with transmitter keyed and verify that 100% modulation capability is obtained.

STEP 3

Connect counter through 10X probe to wattmeter load and check the transmit frequencies on all channels.

SYNTHESIZER

STEP 1

Check voltage on emitter of Q26 for 4.8-5.4 VDC and TP3 for about 2.7 VDC. If not see Fig. 5-12.

STEP 2

Check waveform at the collector of Q23. If waveform is not present or is substantially reduced in amplitude, go to Fig. 5-12. If waveform appears normal, go to Step 3.

STEP 3

Monitor the output frequency of the syntheziser at the collector of Q23 (coupled to the counter with the 10X oscilloscope probe) in both transmit and receive modes. Check to see that the output frequency on each channel agrees with the frequencies listed in Table 5-5. If the output frequencies are wrong in either mode, on any channel, refer to Table 5-14.

FIG. 5-3 TRANSMITTER TEST CONNECTION

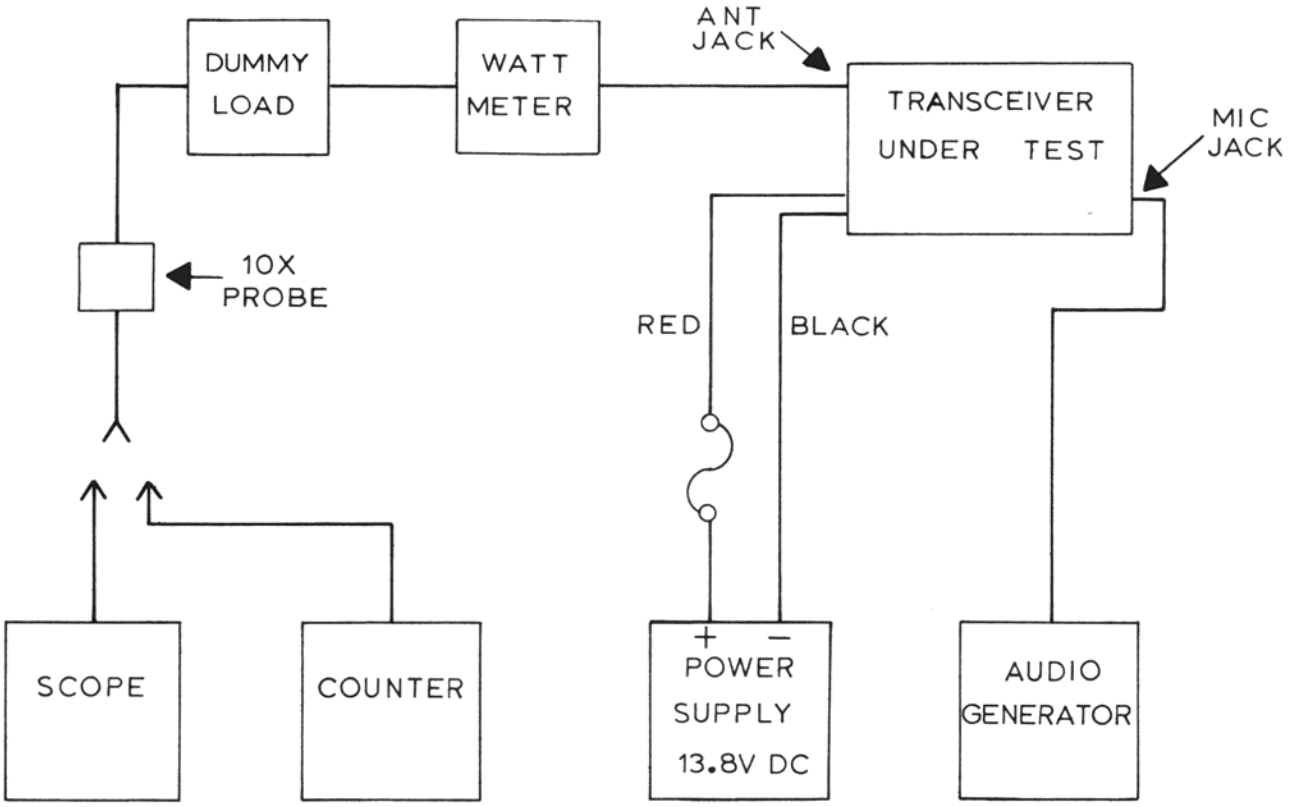


FIG. 5-4 RECEIVER TEST CONNECTION