8, therefore it's recommended that when the disabler circuit appears to be operating without cause, the following procedures should be followed: First, one lead of C502 should be removed, if this allows the disabler circuit to turn off and the transmitter and receiver to operate normally, with phase lock being maintained, probably either I.C. 8 or I.C. 9 is defective. The simplest approach is to replace I.C. 8. If this does not solve the problem, then replacing I.C. 9 should do so.

A condition where the transmit or receive frequency of the synthesizer is off by 460 KHz will sometimes occur in the synthesizer. This can generally be narrowed down to either an open D13, an open R530 or a defective I.C. 4. The voltage at pin 10 of I.C. 4 should be approximately 7/10 of a volt in the transmit mode and approximately 4 volts in the receive mode. If these conditions are present and yet the frequency is still off by 460 KHz in one mode or in the other, I.C. 4 can be assumed to be defective.

Locating a defect in the programmable divider which results in an incorrect division frequency, should consist of the following procedure: First, the programming defects chart should be compared with the actual frequency differential present to determine if the defects on the programming input lines may be the problem.

The next step is to assess whether the division ratio defect is present both on transmit and receive or is present only in one of the two modes. Defects present in only one of the two modes will almost always be due to D13, R530 or I.C. 4. In rare cases, a defect in the binary outputs of one of the counters (Q_0 through Q_3) can also cause this effect, however, the above mentioned components should always be checked or replaced first.

Generally, defects in I.C. 1 will account for 10 KHz to 80 KHz errors in divider output. Defects in the programming inputs to I.C. 2 or 3 or internal defects in I.C. 2 or 3 will almost always cause a loss of phase lock due to a very large change in the total division ratio, resulting in a desired oscillator frequency far beyond the capability of the oscillator.

A simple way to determine the approximate division ratio is to note the oscillator frequency. (The oscillator frequency may be set to some convenient value by grounding test point 3 and adjusting L14 to a suitable frequency or driving test point 3 with a variable 1-4 volt power supply output to set it to approximately the correct frequency.) After this is done, the output frequency of the divider may be measured and the approximate division ratio determined. The scale of the error in division will indicate which chip is likely to be causing the problem. Small errors are usually the result of defects in I.C. 1, larger errors in I.C. 2, and extremely large errors in I.C. 3.

The division ratio of I.C. 3 is unchanging at 7 to 1, therefore, when the output of the divider circuit is 10 KHz, the input to I.C. 3 is always 70 KHz.

NOTE: Division ratio equals input frequency divided by output frequency, for example: channel 13 receive division ratio is 1,642.

$$\frac{16{,}420\ \text{KHz}}{10\ \text{KHz}} = 1{,}642$$

4. T.T.L. LOGIC LEVELS

The microcircuits used in the programmable divider of the SBE-26CB utilize a form of logic circuitry known as T.T.L. (an acronym for Transistor-Transistor Logic). In general, T.T.L. circuitry is direct coupled. This means that DC levels as well as AC voltage swings are important in determining whether or not an input or output of a T.T.L. gate is satisfactory. All T.T.L. logic is designed with standard compatible inputs and outputs so that gates may be interconnected without external interface devices.

The operational states of an input or output in a T.T.L. system, operating normally, have two possible conditions. The first of these is "logical zero", "low" or simply "zero". In standard T.T.L. logic this is defined as an input or output gate having a voltage less than +.8 volts relative to ground. In other words, when an output of one T.T.L. gate drives another gate to less than .8 volts relative to ground, you can be sure that the input gate recognizes the signal as a logical zero or low input. Conversely, a "logical one", "high" or simply "one" is defined as a voltage on any input or output greater than +2 volts relative to ground. In other words, whenever an input is driven to greater than 2 volts relative to ground, it will always recognize this as the logical one state.

The above specifications for the two logic states are "worst case" conditions. This merely means that under the worst possible conditions of external noise, tolerances in power supply voltage and extremes of temperature (within ratings), any input gate will always recognize inputs meeting the above specifications.

Therefore, under optimum operating conditions (25°C temperature, exactly 5 volts supply voltage and no problems with external noise) these limits for logical zero and logical one can usually be exceeded somewhat. Generally, one can expect a T.T.L. gate to recognize anything from about 1.1 volts or lower as a logical zero and anything from about 1.6 volts or higher as a logical one. Of course, it is generally preferable to stay within the worst case conditions for input voltages to insure that the best possible performance under all operating conditions can be met.

From the above it can be seen that the most important point to assess when determining if a drive signal to a T.T.L. gate is satisfactory, is to determine whether the positive and negative peaks of the drive signal are driving the gate input to sufficiently high and low levels, to meet worst case conditions.

Occasionally, if drive is marginal to a T.T.L. gate, for instance if the drive from Q25 to the programmable divider chain is marginal, operation may be normal while the unit is cool and abnormal after the temperature rises due to normal heating of the transceiver in operation. Again, under these marginal conditions, a variation in supply voltage within normal specifications may result in improper operation under certain conditions when T.T.L. drive levels are only being marginally met.

It is important to realize that many symptoms that may appear to be intermittent due to a loose connection or an otherwise mechanically induced malfunction, may in fact be due to marginal drive to the divider circuitry, resulting in intermittent operation.

LOSS OF PHASE LOCK

1. Check for 5 volts ±10% at the emitter of Q26.	Voltage OK: Go to Step 2. Wrong voltage: D27, Q26, C528 or R529 defective or excessive loading on 5 volt line. (Disconnect loads in turn and check for shorts.)
2. Check the wave-form at the collector of Q24.	Normal wave-form: Go to Step 4. Abnormal wave-form: Go to Step 3.
3. Check the wave-form at the emitter of Q9 (Reference Oscillator).	Normal wave-form: Q24 or associated circuitry defective, or excessive loading from I.C. 5. Abnormal wave-form: Q9 or associated circuitry defective.
4. Check the wave-form at the emitter of Q21.	Normal wave-form: Go to Step 5. Q21 oscillator circuit including D26, L14, C509, R508, etc.
5. Check the wave-form at the emitter of Q25.	Abnormal wave-form: Q25 or associated components defective or excessive loading from I.C. 1, 2 or 3. NOTE: Excessive loading from the I.C.'s may be checked by carefully de-soldering pin 2 of each I.C. in turn, thus removing the loading.
6. Check the wave-form at pin 1 of I.C. 9.	Wave-form greatly distorted or not present: Defect in I.C.'s 5-8. Locate individual I.C. at fault by measuring input and output wave-forms and frequencies of each I.C. in turn. (An I.C. with the correct input and wrong output may be assumed defective.)
7. Measure wave-form at pin 3 of I.C. 9.	Normal wave-form: Go to Step 8. Wave-form distorted or absent: I.C.'s 1-4 defective.
8. Clamp V.C.O. with +2.5 volts DC at TP-3. (Either a highly regulated supply or a battery should be used.) Adjust L14 for 17 MHz. Varying the clamp voltage between 2 and 3 volts should produce an oscillator frequency shift of more than 1 MHz.	No response or wrong frequency range: D26, Q21 or associated circuitry defective. Test OK: Problem is in I.C. 9, Q20 or associated circuitry.

PROGRAMMING DEFECT SYMPTOMS

PROGRAMMING DEFECT	CHANNELS AFFECTED	SYMPTOM
S_0 Stays Low	2, 5, 7, 8, 10, 13, 15, 16, 18, 21, 23	10 KHz High
S_0 Stays High	1, 3, 4, 6, 9, 11, 12, 14, 17, 19, 20, 22	10 KHz Low
S_1 Stays Low	1, 4, 7, 10, 11, 13, 14, 16, 17, 20	20 KHz High
S_1 Stays High	2, 3, 5, 6, 8, 9, 12, 15, 18, 19, 21, 22, 23	20 KHz Low
S_2 Stays Low	1, 2, 3, 7, 8, 9, 13, 14, 15, 20, 21, 22	40 KHz High
S_2 Stays High	4, 5, 6, 10, 11, 12, 16, 17, 18, 19, 23	40 KHz Low
S_3 Stays Low	1, 2, 3, 4, 5, 6, 13, 14, 15, 16, 17, 18, 19	80 KHz High
S_3 Stays High	7, 8, 9, 10, 11, 12, 20, 21, 22, 23	80 KHz Low
S_4 Stays Low	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	160 KHz High
S_4 Stays High	13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23	160 KHz Low

Defects resulting in incorrect programming inputs to the first two integrated circuits of the programmable divider (I.C. 1, I.C. 2) will result in characteristic failure symptoms. The possible failures and their associated failure symptoms are charted above.

If the transmit and receive frequency is high or low by one of the amounts stated above on certain channels, check to see if the channels affected correlate with one of the groups shown on the chart above. A correlation between the symptom chart and the actual defect in the radio can, in this way, narrow down a failure to a specific section of the channel selector switch, its associated pull up resistor, and the I.C. to which it is connected.

5.4 RECEIVER SERVICING

Unless otherwise noted, the front panel controls should be set as follows: Set the LOC/DIS switch on the front panel to the distance position and adjust the volume control to maximum, clockwise, set the delta tune control to the center position, set the CB/PA switch in the CB position, set the noise limiter switch in the off position, turn the squelch control fully counterclockwise, set the channel selector on channel 13. Connect the transceiver to a 13.8 volt DC power supply.

No Receive

1. Connect the signal generator to the entenna jack. Inject a high level modulated signal at the channel frequency. (Approximately 10,000 microvolts.) Check for "S" meter deflection.

   "S" meter deflects: Go to Step 2.
   "S" meter does not deflect: Go to Step 8.

2. Check internal speaker by plugging in an external unit. Check for audio while the signal generator is set up as in Step 1.	If audio from the test speaker is normal, the internal speaker or R215 is open.
3. With the signal generator set up as in Step 1, check for audio at test point 4 (transmitter).	Good audio at test point 4 indicates a probable defective relay, CB/PA switch, external speaker jack or associated wiring. No audio at test point 4, go to Step 4.
4. Check the emitter voltage of Q14.	Approximately 2 volts, go to Step 5. If the result is approximately 3.2 volts, the problem is in the squelch circuit. (Refer to section 4.1, Squelch.)
5. Set the CB/PA switch to the PA position. Connect an external speaker to the P.A. jack, plug in the standard microphone. Key the microphone and determine if the P.A. system is working normally. NOTE: The microphone gain control should vary the output in the P.A. mode.	P.A. function OK. Probable receiver fault is in the detector A.N.L. or tone control circuit. Go to Step 6. No P.A. function. Problem is in audio amplifier chain. Go to Step 7.
6. Locate defect in the audio detector, A.N.L. or tone control circuit by signal tracing through the circuitry with the signal generator connected as in Step 1.	
7. Check for defect in audio amplifier chain by either signal tracing with an oscilloscope with the generator connected as in Step 1, monitoring the audio output while injecting audio from a test oscillator, or making DC tests and comparing voltages to those listed on the schematic.	Defect is probably Q14, Q15, Q16, Q17 or associated components.
8. Check receive bus at cathode of D5 (9 volts ±10%).	If voltage is low or zero, suspect shorted D5, C123 or C114. Open R701 or excessive bus loading. If 9 volt line is OK, go to Step 9.
9. Check the voltage at test point 1 with no signal. (Approximately .7 volts)	If voltage is zero, suspect open R107, shorted C126, or open Q1. If test point 1 voltage is normal, go to Step 2.

Weak Receive

NOTE: If any evidence of tampering with the unit is found, perform the alignment procedure as outlined in section 6.1.

1. Refer to receiver injection chart and isolate weak stage by injecting at detector and pro-

gressing back through the receiver chain to the front end.

NOTE: Although the synthesizer performance verification indicates normal output from the reference oscillator and synthesizer output buffer, injection to the mixers should be verified.

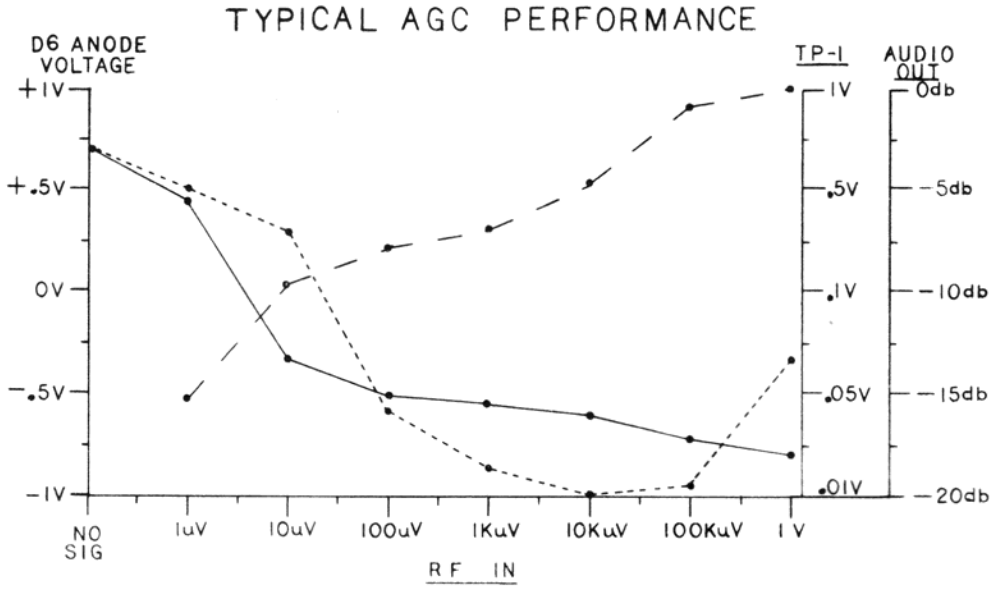
FIG. 5.4-1 RECEIVER INJECTION CHART

The following injection signals should produce approximately four volts audio output. All signals are modulated with 1 KHz @ 30% (audio output is terminated in 8 ohms).

Squelch is fully counter-clockwise, volume is at maximum, LOC/DIS switch is in distance position, and tone control is at mid-position.

INJECTION POINT	INJECTION LEVEL	FREQUENCY
Anode of D2	2 microvolts	Channel Frequency
Collector of Q1	60 microvolts	Channel Frequency
G_2 of Q2	40 microvolts	Channel Frequency
Drain of Q2	600 microvolts	10.695 MHz
TP2	100 microvolts	10.695 MHz
Base of Q3	40 microvolts	455 KHz
Collector of Q3	.01 volts	455 KHz
Base of Q4	700 microvolts	455 KHz
Collector of Q4	.7 volts	455 KHz
Anode of D9	1 volt	455 KHz

FIG. 5.4-2 AGC PERFORMANCE GRAPH



5.5 TRANSMITTER SERVICING

No Carrier

1. Check for relay action with keying.	If relay fails to pull in, check or replace microphone, check relay and associated circuitry.
2. Check for approximately 13 volts at test point 4.	13 volts missing, check D19 and T9 secondary for opens.
3. Perform synthesizer performance verification. (Section 5.2)	If synthesizer performance is verified as normal, continue with **Weak Carrier** section of the Transmitter Service Procedure.

Weak Carrier

NOTE: If there is any evidence of misalignment, perform the alignment procedure as outlined in Section 6.2 before continuing with this procedure.

1. Check DC voltages on Q5, Q6, Q7 and Q8 in the transmit mode.	If any voltages are substantially abnormal, make further checks in the stage involved.

2. Refer to the wave-form keys on the schematic. Check the transmitter wave-forms to isolate the defective stage.	Check Q5 through Q8.

NOTE: Tuned impedence matching networks couple R.F. between transmitter stages. Substantial "de-tuning" of one of these stages can result in very low or no output. Defects causing this effect can include shorts, opens or severe value changes in either the series or shunt reactances.

A wave-form with abnormally high peak to peak value often indicates a defect in the following stage or the intercoupling network.

Remember that low stage gain can also be caused by open bypass capacitors such as C405, C409 or C410.

A good method for discovering de-tuned, nonresonating coupling circuits, is to tune the associated coils through their normal range, if no "peak" is found, you may probably assume that the circuit is not resonating. Remember that "Q" of many of these stages is fairly low. Therefore, the peak may be rather broad, especially, in the output coupling network.

FIG. 6.1-1

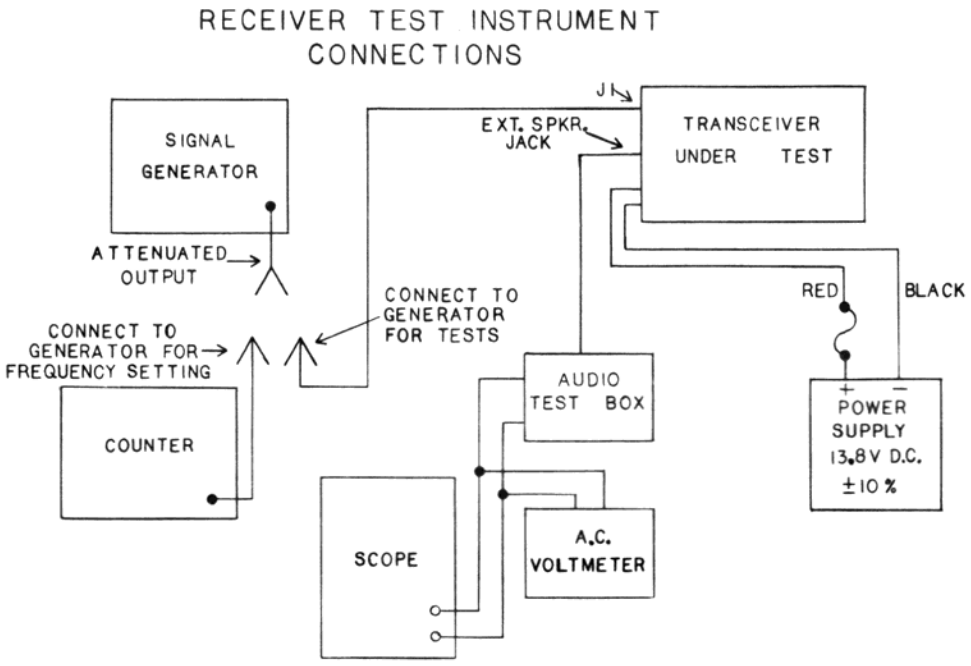
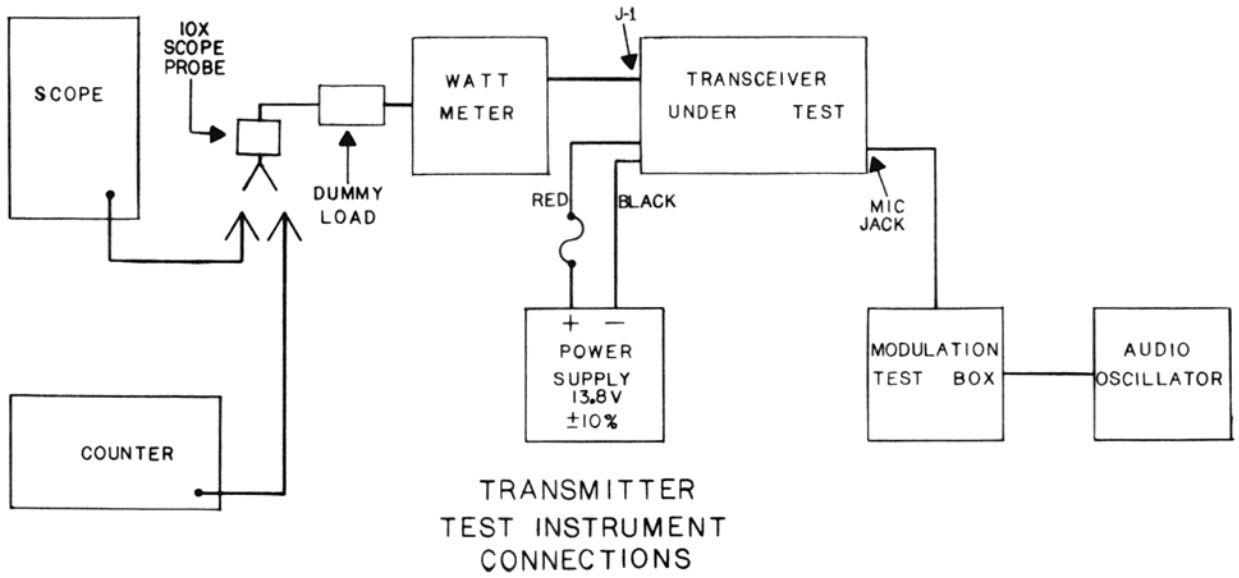


FIG. 6.2-1



SECTION 6
ALIGNMENT

RECEIVER ALIGNMENT PROCEDURE

INITIAL SET-UP

Connect the test equipment to the unit as shown in figure 6.1-1. Set the local-distance switch on the front panel to the distance position. Adjust the volume control to maximum, clock-wise. Set the delta tune control to the center position. Set the CB/PA switch in the CB position. Set the noise limiter switch in the off position. Turn the squelch control fully counter clock-wise. Set the channel selector on channel 13.

STEP 1

Set the output level of the signal generator to a level sufficient to provide 3 volts of audio as measured on the audio voltmeter. Adjust in turn the following: T1, L1, T2-1, T2-2, T3, T4, T5, and T6 for maximum indication on the voltmeter. If at any time during the alignment procedure the audio level increases to more than 5 volts, reduce the generator output level to result in an audio output level of 3 volts.

STEP 2

Repeat the above procedure until a nominal 5 volts or more is available at the audio output with an input of 1 microvolt.

STEP 3

Adjust the audio output level with the volume control to result in a reading of 0db on the voltmeter. Adjust the slug of T1 counter-clockwise for a reduction of 1db in audio output. Remove the generator input from J1. Adjust the volume control to obtain a useable reading of the background noise level. On the voltmeter, switch the channel selector to channel 1 and note the noise level. Switch to channel 23. The noise level should be within 2db of the channel 1 reading. If the difference between 1 and 23 is greater than 2db, adjust L2, slightly to reduce the differential.

STEP 4

Set the generator output to 100 microvolts. Adjust VR7 for a reading of "9".

STEP 5

Rotate squelch control fully clockwise. Increase generator output to 300 microvolts. Squelch should break. If squelch fails to break, adjust VR8 to break squelch at 300 microvolts.