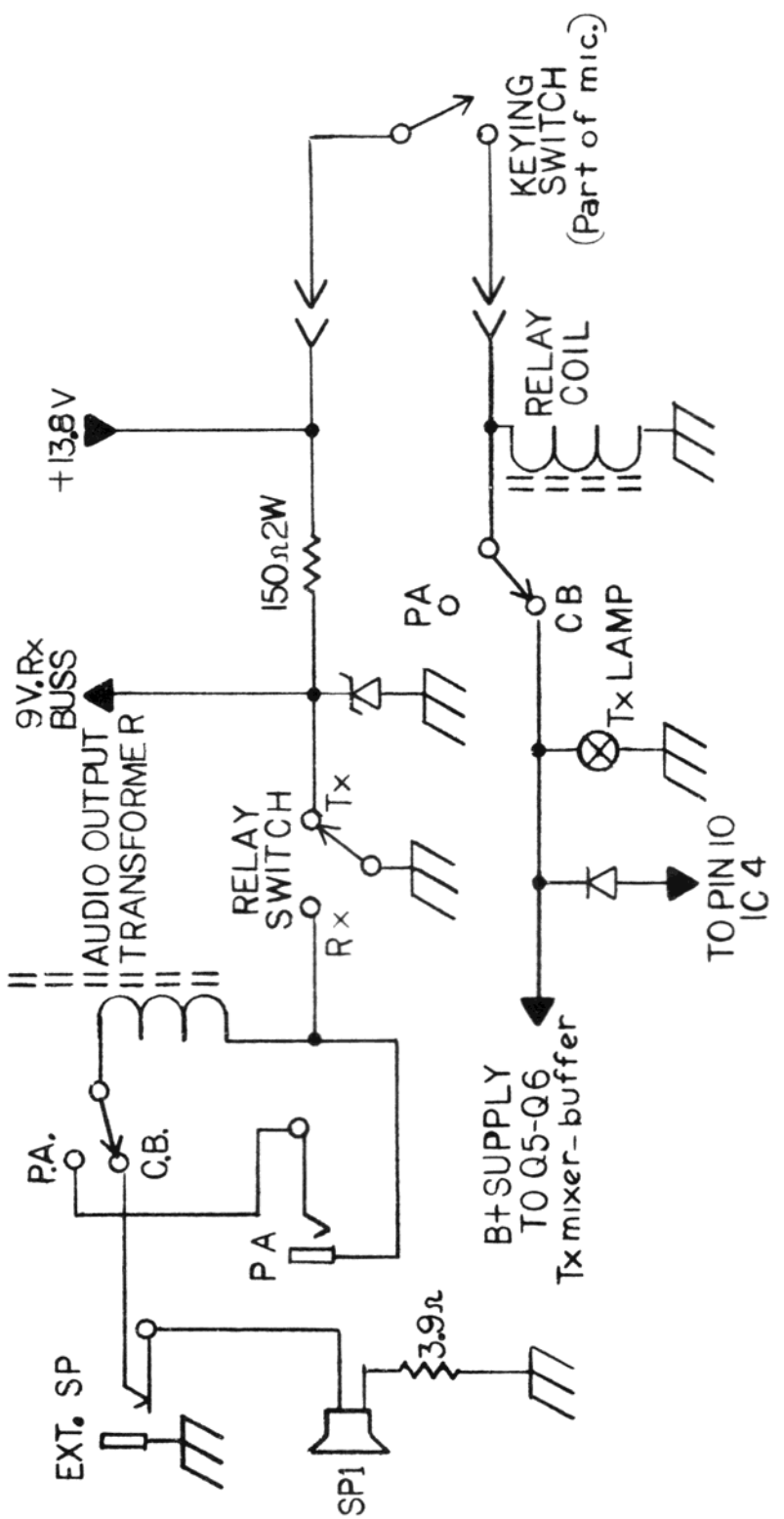
FIG. 4.3-1 TRANSMIT-RECEIVE SWITCHING



4.3 TRANSMIT-RECEIVE SWITCHING CIRCUITRY

The transmit to receive switching circuitry of the SBE-26CB utilizes a single pole, double throw relay. This relay serves two functions. In the transmit mode, it shunts to ground the 9 volt receiver B+ supply. In the receive mode, it provides a ground return for the audio output winding of T9, the audio output/ modulation transformer.

No switching is used as such between transmitter output and receiver input. Both the receiver input and the transmitter output are continuously connected to the same point. In the transmit mode, damage to the front end of the receiver is prevented by the action of D2. D2 is connected to the primary side of T1, which is the receiver R.F. input transformer. In the receive mode, it is reverse biased by the 9 volt receive bus and has no effect on performance of the receiver. However, in the transmit mode this bias is removed. This allows D2 to shunt to ground through C104, any large amplitude signals arriving from the transmitter. This, plus the impedence of C101, the 20pf coupling capacitor, protects the receiver against the large voltages present at the output of the transmitter.

The high level modulated B+ supply to the final and driver is not switched, and therefore, audio output from the receiver appears on this line in the receive mode. However, the B+ supply to the transmit mixer and the transmit buffer is supplied only when the microphone is keyed.

Pin 3 of the microphone jack is the unswitched "keyline"; this line is connected directly to the 13.8 volt B+ bus of the radio. Pin 4 of the microphone connector is the switched keyline. It is connected to the relay coil RL1, the transmit-receive relay, a bias circuit for D16, (microphone audio switching diode) and passes through the CB/PA switch, supplying voltage to PL1, the transmit light, also supplying B+ to the transmit mixer and buffer.

Keying the microphone shorts the two keylines together, providing 13.8 volts DC to the devices connected to the switched keyline. The microphone element of the standard SBE microphone is not switched. (The element is connected to the "hot" lead of the microphone input at all times.) Therefore, some means is required to remove the audio output of the microphone from the base of the audio amplifier "Q14" during the receive mode. This is accomplished by changing the biasing conditions on D16. During the transmit mode, D16 is forward biased by means of a bias circuit operating from the switched keyline consisting of R217, R218 and R204 in the base circuit of Q14. In the receive mode, the switched side of the keyline goes to ground, which removes the forward bias from D16, turning it off and removing the microphone audio from the base of Q14. The detector output of the receiver is connected directly to the base of Q14, through the volume and tone control circuits. No switching is necessary on this line, because the receiver is totally disabled on transmit by the shorting of the 9 volt receive bus to ground by RL1.

4.4 SYNTHESIZER

The synthesizer in the Formula D is of the indirect type. In this form of synthesizer a voltage controlled oscillator's output is compared in frequency to that of a highly stable crystal oscillator. To be more specific, the ratio of the two frequencies is compared (the stable reference oscillator's frequency need not be the same as that of the voltage controlled oscillator). The ratio of the frequency of the voltage controlled oscillator to that of the reference oscillator is set by "programming" the divider cicruitry internal to the synthesizer.

The circuitry of the Formula D synthesizer can be divided into seven sections. These are discussed in the following paragraphs.

REFERENCE OSCILLATOR

This is the only crystal controlled oscillator used in the Formula D. It provides the only frequency reference for the entire radio. The reference oscillator operates on a frequency of 10.240 MHz on receive and 10.2381 MHz on transmit.

REFERENCE DIVIDER

This is a divider circuit consisting of I.C.'s 5, 6, and 7 the purpose of which is to perform a division of the reference oscillator frequency by 1,024 to 1. This results in an output frequency of 10 KHz on receive and 9.9981 KHz on transmit.

VOLTAGE CONTROLLED OSCILLATOR

This section of the synthesizer provides the actual output signal at a frequency of 16.27 to 17.017 MHz. Its frequency is controlled by a D.C. input voltage provided by other circuitry in the synthesizer, which maintains its stability to crystal accuracy.

PROGRAMMABLE DIVIDER

The programmable divider serves the function of dividing the output frequency of the V.C.O. in such a manner as to result in an output frequency that is the same as that of the reference divider's output when the voltage controlled oscillator is operating at its correct frequency. To allow the V.C.O. to operate at a large number of different frequencies, the division ratio of this divider is variable.

PHASE DETECTOR

The phase detector in the SBE-26CB synthesizer is a section of I.C. 9, the MC4044 integrated circuit. The phase detector's function is to compare the two inputs for their phase relationship. These two inputs are the output of the reference divider and the output of the programmable divider. When the phase, and therefore the frequency, of the programmable divider's output varies from that of the reference divider, the phase detector acts to take corrective measures to return the V.C.O. frequency to its proper value.

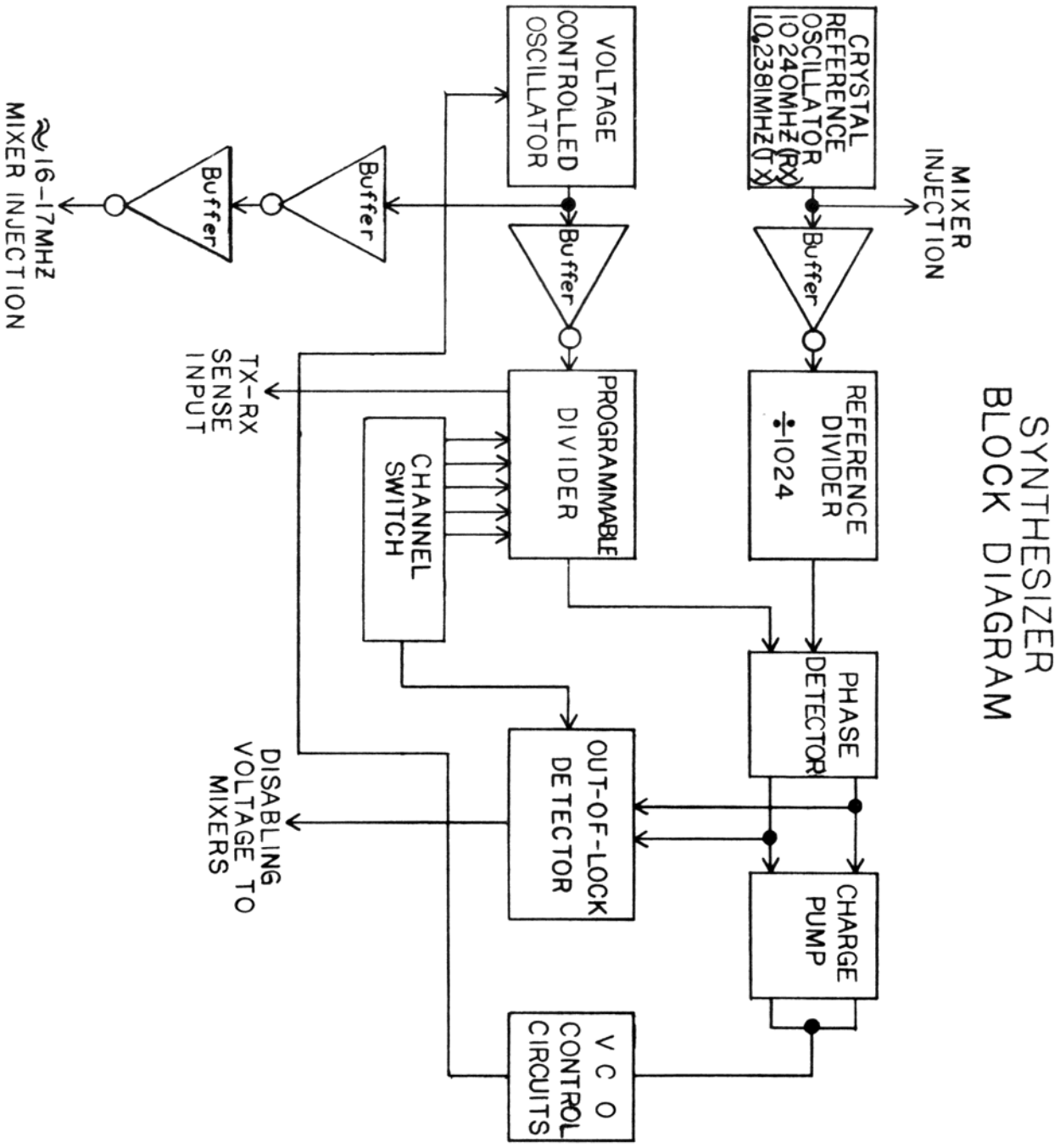
CHARGE PUMP

The charge pump is also a section of I.C. 9. The function of this circuit is to translate the phase detector output to a form suitable for driving the V.C.O. control circuitry.

CONTROL CIRCUITRY

The control circuitry of the synthesizer consists of an additional section of I.C. 9 and associated circuitry which will be explained in detail later in this description. This circuitry performs the function of translating the charge pump output into a suitable control voltage for use in setting the voltage controlled oscillator frequency.

FIG. 4.4-1


SYNTHESIZER
BLOCK DIAGRAM
CRYSTAL
REFERENCE
OSCILLATOR
10.240MHz (RX)
10.238MHz (TX)
MIXER
INJECTION
Buffer
REFERENCE
DIVIDER
÷1024
PHASE
DETECTOR
CHARGE
PUMP
V C O
CONTROL
CIRCUITS
VOLTAGE
CONTROLLED
OSCILLATOR
Buffer
PROGRAMMABLE
DIVIDER
CHANNEL
SWITCH
OUT-OF-LOCK
DETECTOR
DISABLING
VOLTAGE TO
MIXERS
TX-RX
SENSE
INPUT
Buffer
Buffer
≈16-17MHz
MIXER INJECTION

OUT OF LOCK DISABLE CIRCUIT

This section of the synthesizer insures that any improper output frequency from the synthesizer will be ignored by the radio. This is done by detecting the "out of lock" condition and generating a voltage which is used to disable the receiver and transmitter mixers.

PHASE DETECTOR CIRCUIT DESCRIPTION

General Description

No attempt will be made to describe the internal functioning of the phase detector used in the Formula D, as considerable knowledge of digital devices is required to grasp its mode of operation. Furthermore, understanding its operation is not required of the technician servicing the synthesizer. We will confine our description to the external effects of its normal operation.

The input of the phase detector is at pins 1 and 3 of the MC4044 I.C., which is shown on the schematic of the Formula D as I.C. 9. The outputs of the phase detector are pins 13 and 2.

Normal Operation

Operation of the phase detector is as follows: Two signals are applied to it, the reference divider's output to pin 1 and the programmable divider's output to pin 3. The internal circuitry of the phase detector compares the phase relationship of the negative going transitions of the pulses from the reference divider and the programmable divider.

In the normal operation of the phase detector, very narrow negative going pulses will occur at both phase detector outputs at 100 microsecond intervals. Should the voltage controlled oscillator drift slightly, the output pulses of the phase detector associated with the direction of the drift will widen (stay negative longer). For example, should the output of the V.C.O. tend to drift downward in frequency, the "lagging" output pulses of the phase detector will widen.

The voltage controlled oscillator will normally drift continually while the radio is in operation. This means that the small phase corrections from the phase detector will occur continually at 100 microsecond intervals, during normal operation.

Loss of Phase Lock

Loss of phase lock is described as a condition under which it is not possible for the control circuitry to alter the oscillator frequency sufficiently to bring the inputs to the phase detector at pins 1 and 3 into phase coincidence.

When the phase detector of I.C. 9 is operating normally, a loss of phase lock will result in a wide pulse from one of the phase detector outputs. This pulse will occur continually at 100 microsecond intervals. In other words, a considerable phase difference is detected by the phase detector, but the control range of the associated circuitry is, for some reason, not sufficient to bring the oscillator to the correct frequency.

A continuous train of wide pulse will occur at the leading output (pin 2) of the phase detector when an uncorrectable difference in phase at its two inputs occurs, such that the V.C.O. divider output frequen-

cy is higher than the reference divider frequency (the V.C.O. divider pulses lead the reference divider pulses in phase when their negative going transitions are compared by the phase detector). Conversely, a continuous series of wide pulses from the lagging output at pin 13 will occur when the V.C.O.'s divider frequency is lower than that of the reference divider (lagging reference divider in phase).

CHARGE PUMP CIRCUIT DESCRIPTION

General Description

The purpose of the charge pump is to change the negative going pulses at the two outputs of the phase detector to either positive or negative going pulses suitable for input to the circuitry that follows. The charge pump can be divided into two segments. Each segment couples one input to a common output.

Leading Input

This section of the charge pump is connected to the leading output of the phase detector. Although its circuitry is fairly complex, it can be thought of as an inverter followed by a diode (see diagram). The effect of this section of the circuit is to invert the input pulse from the leading output of the phase detector and couple it to the output in such a manner that only when the output of the inverter is more positive than the voltage at the common output are the two connected, otherwise the diode is back biased, effectively isolating this input from the common output.

Lagging Input

This input of the charge pump is very simple and obvious in operation. It merely consists of a diode connected with its cathode to the input and anode to the common output so that only when the lagging input is more negative than the common output, are they connected together. Otherwise, the diode isolates the lagging input from the common output.

Normal Operation

When the synthesizer is in phase lock, the normal inputs to the charge pump will be two very narrow pulses from the phase detector, both of which occur at the same time and at 100 microsecond intervals. Under these conditions, a D.C. voltage will appear (provided by external circuitry, which will be explained later) at the common output of the charge pump at pins 5 and 10. Reference to the block diagram will show that between the negative going pulses of the phase detector output, both of the coupling circuits in the charge pump will be in an isolating condition (both diodes will be back biased). Therefore, in practical terms, the common output of the charge pump is totally isolated from both inputs when the inputs are at logical 1. However, if a negative going pulse occurs on one of the inputs, the common output will have coupled to it either a negative going or positive going pulse, depending upon which input received the pulse from the phase detector. To reiterate, when a pulse occurs on the leading input, a positive going pulse appears on the output; when a pulse appears on the lagging input, a negative going pulse appears on the output. During the time when no pulses occur at either input to the charge pump, the common output is totally isolated from both inputs.

VCO CONTROL CIRCUIT DESCRIPTION

General Description

The basic purpose of this circuit is to provide a stable DC output voltage for the control of the voltage controlled oscillator which can be quickly altered as conditions require, by the action of the charge pump. The basic form this circuit takes is that of an inverting amplifier with its output capacitively coupled back to its input. This inverting amplifier has a very high current gain and therefore, although its output impedence is low, its input impedence is very high. This means that the relatively small capacitor (1 microfarad) connecting the input to the output can be used as a "memory", in other words, the charge across this capacitor sets the differential voltage between the input and the output. Therefore the output voltage of the amplifier is strictly dependent upon the charge of this capacitor. The circuit is coupled in such a way as to allow the output of the charge pump to vary the charge on C507.

Circuit Description

A one microfarad electrolytic capacitor (C507) is connected at its cathode end to the base of an emitter follower stage which is shown on the schematic diagram as Q20. The purpose of this emitter follower is simply to make the impedence at the cathode of C507 very high. The output voltage of the emitter follower directly tracks the voltage at the cathode of C507 and it drives the input of the last section of the MC4044 chip which consists simply of a Darlington DC amplifier. This amplifier greatly amplifies and inverts whatever voltage changes occur at the base of Q20. The output of this amplifier is connected to the anode end of C507 through a resistor of small value which for the moment can be discounted. Also connected to the cathode of C507 and the base of Q20 is an R-C filter network consisting of R505, R506 and C506. The other side of this low pass filter network is coupled to the output of the charge pump at pins 5 and 10. The purpose of this filter is to slow the rise time of the output pulses from the charge pump and also to reduce their value to a low enough level to insure against over reaction from the control circuitry which would result in oscillation of the system. The output of the control circuitry is taken at pin 8 of I.C. 9 and passes through R519, a 2.2K isolating resistor, to the cathode of D26, the varactor diode, used as the variable capacitance in the voltage controlled oscillator.

Normal Operation

It can be seen that the voltage appearing on the input of the inverting amplifier (base of Q20) is dependent upon the charge across C507. It is also obvious that the output voltage of the inverting amplifier is directly related to the input voltage. Therefore, the charge across the capacitor sets the output voltage of the inverting amplifier and therefore the DC control voltage to the V.C.O. Due to the fact that the high impedence of the inverting amplifier offers little loading to the capacitor, the charge across the capacitor will tend to remain stable for reasonably short periods of time, and therefore the output voltage of the amplifier will also tend to remain stable.

Control of the output voltage is affected by changes in the charge across C507, which are forced to occur by the action of the charge pump's output.

The charge pump controls the charge across C507 and therefore the output voltage of the V.C.O. control circuit in the following manner: Assume that the output frequency of the voltage controlled oscillator is slightly low. This will result in a narrow pulse from the leading output of the phase detector and a much wider pulse from the lagging output of the phase detector. The leading output of the phase detector will be inverted by the charge pump and the lagging output will be coupled through as a negative pulse. Due to the fact that the negative going "lagging" output pulse is much wider than that of the leading output, they will not cancel each other out completely at the common output of the charge

pump. The net effect will be a negative going pulse to the output of the charge pump which, after being reduced in amplitude by the integrator, will tend to cause a slight reduction of the base voltage of Q20. This will result in a still small but amplified positive change in the output voltage of the control amplifier. This will, of course, tend to slightly increase the charge across C507. This will result in the control circuit stabilizing at a slightly higher output voltage. This process is repeated at 100 microsecond intervals until such time as the voltage at the output of the control circuit reaches a sufficiently high level to bring the oscillator frequency to its proper value and allow phase lock to be regained. The exact same set of circumstances will reoccur if the oscillator frequency becomes too high. The only difference being that the polarities of the voltage changes will be reversed.

VOLTAGE CONTROLLED OSCILLATOR CIRCUIT DESCRIPTION

The voltage controlled oscillator of the Formula D synthesizer consists of Q21, D26 and associated circuitry. The oscillator circuit is of the common collector variety, with its output frequencies set by the resonance of a tank circuit consisting of D26 and L14. D26 is a voltage variable capacitance diode. It is operated with a variable reverse bias, which is provided by the output of the V.C.O. Control Circuits through R519.

When the reverse bias voltage on D26 is increased, its capacitance decreases. Conversely, when the bias voltage is reduced, the capacitance of the diode increases. An increase in capacitance in the tank circuit will tend to reduce the oscillator frequency and a decrease in capacitance in the tank circuit will tend to increase the frequency. Therefore, as the bias voltage rises, the frequency of the oscillator will also rise.

The output of Q21 forms the synthesizer's output signal after being amplified by two stages of buffer amplification (Q22 and Q23). The output of Q21 at its emitter is also used to directly drive the programmable divider input amplifier (Q25).

FIG. 4.4-2 OSCILLATOR CONTROL -- OUT-OF-LOCK DETECTOR

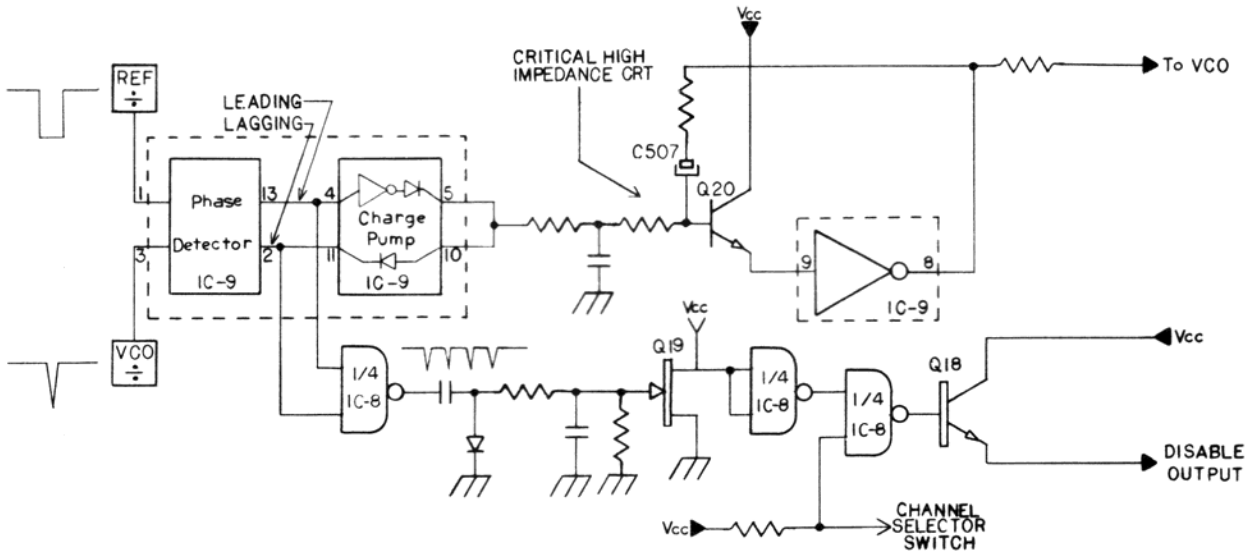
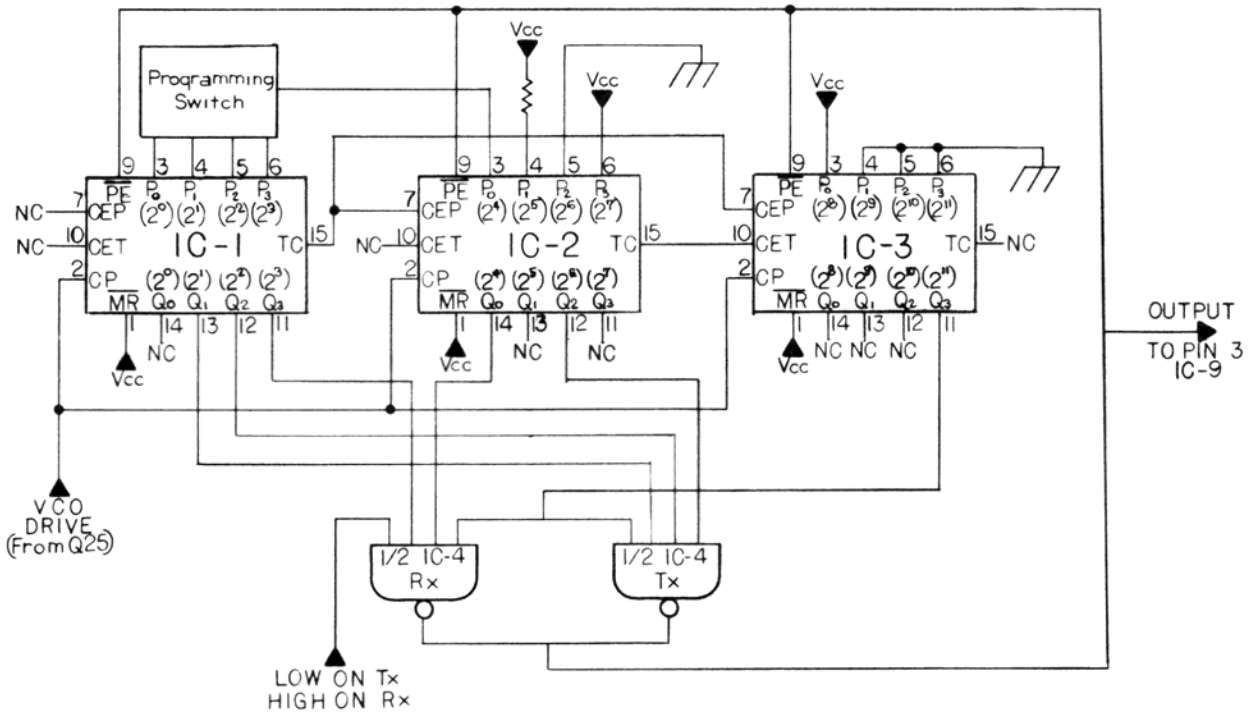


FIG. 4.4-3 PROGRAMMABLE DIVIDER LOGIC DIAGRAM



PROGRAMMABLE DIVIDER CIRCUIT DESCRIPTION

General

The programmable divider consists of four integrated circuits, I.C. 1, I.C. 2, I.C. 3 and I.C. 4. The purpose of this circuit is to provide a division of the voltage controlled oscillator output, such that when the oscillator is operating at the proper frequency, the programmable divider's output will be equal in frequency and phase to the output of the reference divider.

The V.C.O. must operate at a total of 46 different frequencies. This necessitates that the division ratio of the programmable divider be changeable so that all desired V.C.O. frequencies will result in the proper output frequency from the divider.

A complete description of the internal operation of the programmable divider is beyond the scope of this manual. However, a basic description of the operation of the counter follows and should be of assistance to those wishing to study further the operation of programmable dividers.

Circuitry

The programmable divider of the SBE-26CB consists of a three stage circuit employing Fairchild 9316 or Texas Instruments 74163 integrated circuits. These I.C.s are four-bit binary counters with programming capability.