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Realistic TRC-479 (21-1519)

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REALISTIC®

Service Manual

21-1519

TRC-479
40-CHANNEL
CB TRANSCEIVER

Catalog Number: 21-1519

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SPECIFICATIONS

General

Transmitter ---------- Crystal controlled PLL synthesizer, amplitude modulation
Receiver ---------- Crystal controlled double conversion, superheterodyne system
Communication frequencies ---------- All 40 CB channels (26.965 to 27.405 MHz)
Voltage operation ---------- 12 – 16V DC (negative ground vehicles)
Temperature and humidity range ---------- –22° F to +140° F (–30° C to +60° C) and 10% to 90%
Transmitter/Receiver switching ---------- Electrical

Standard Test Conditions

Power supply voltage ---------- 13.8V DC
Signal input level ---------- 1000μV
Modulation frequency and modulation percentage ---------- 1000Hz, 30%
Receiver output power ---------- 500mW at external SP
Receiver output load impedance ---------- 8 ohms, non-inductive
Antenna load impedance of transmitter/receiver ---------- 50 ohms, non-inductive
Measuring channel ---------- 18
Ambient conditions
  Temperature ---------- 77° F (25° C)
  Humidity ---------- 40 to 70% RH

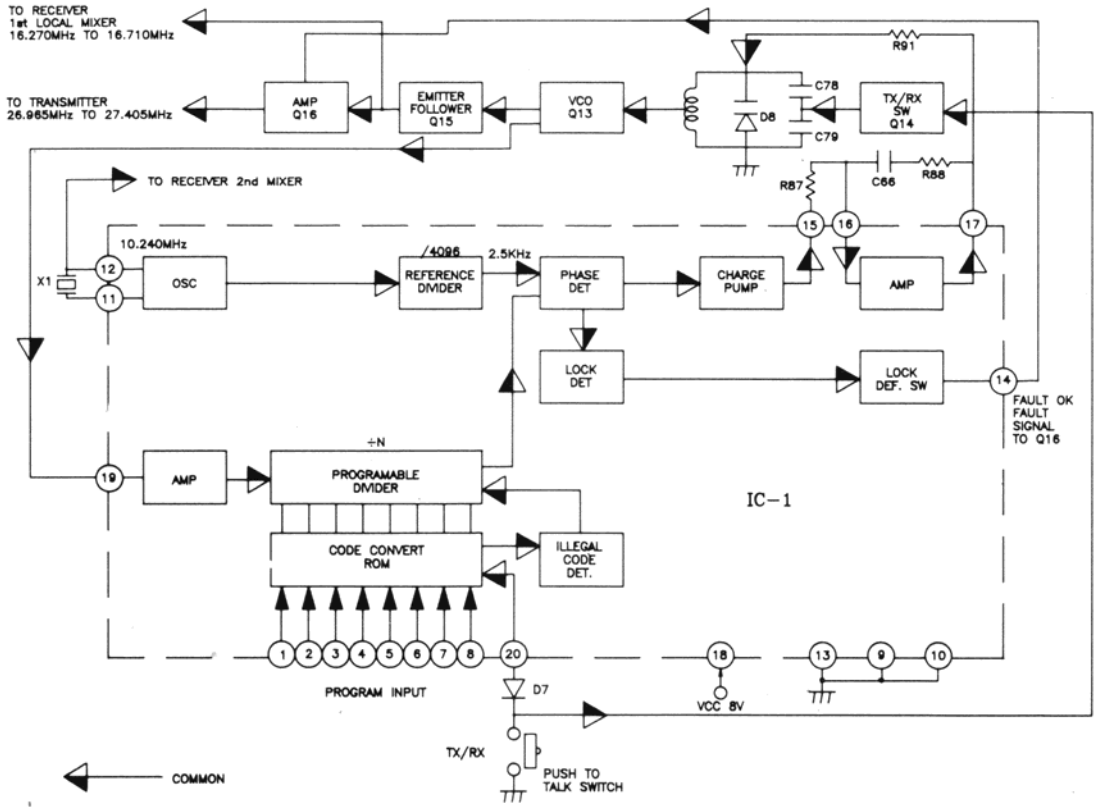
Transmitter		**Unit**	**Nominal**	**Limit**
Frequency tolerance at 77 ° F (25° C) (5 minutes after switch on)		Hz	± 100	± 1300
Carrier power at no modulation		W	3.9	3.6 – 4.4
Modulation attack time		m sec.	18	25
Modulation release time		m sec.	300	300 ± 200
Modulation distortion at 1 kHz 80% modulation		%	3	6
Spurious emission 2nd/3rd/4th/5th/6th 7th/8th/9th/10th		dB	– 70	– 60
Modulation 100% capability positive/negative		%	90	80
Current drain at no modulation		mA	1100	1300
at 80% modulation		mA	1500	2000
Modulation frequency response (1 kHz 0dB reference)				
lower at 450 Hz, EIA		dB	– 6	– 6 ± 3
upper at 2.5 kHz, EIA		dB	– 6	– 6 ± 3
Carrier power uniformity CH to CH at no modulation		W	0.2	0.5
Microphone sensitivity AM for 50% modulation		mV	1.0	2.0
AMC range between 50 to 100% modulation		dB	40	30
Occupied band width	± 5.0 kHz	dB	– 35	– 26
	± 7.5 kHz	dB	– 35	– 26
	± 10.0 kHz	dB	– 45	– 35
	± 12.5 kHz	dB	– 45	– 35
	± 15.0 kHz	dB	– 45	– 35
	± 17.5 kHz	dB	– 45	– 35
	± 20.0 kHz	dB	– 65	– 60
	± 22.5 kHz	dB	– 65	– 60

Receiver	**Unit**	**Nomial**	**Limit**
Maximum sensitivity	μV	0.3	0.6
Sensitivity for 10 dB S/N	μV	0.5	1.0
Squelch sensitivity at threshold	μV	0.7	1.4
at tight	μV	1000	355 – 2820
AGC figure of merit for – 10 dB audio output (Reference RF input 50 mV)	dB	90	70
Overload AGC characteristics from 50 mV to 1V	dB	3	3 ± 6
Overall audio fidelity (1 kHz 0 dB Ref.)			
lower frequency 450 Hz	dB	– 6	– 6 + 3
upper frequency 2500 Hz	dB	– 6	– 6 + 3
Adjacent channel selectivity (±10 kHz)	dB	60	55
Maximum audio output power	W	6.0	4.5
Audio output power at 10% THD	W	5.0	3.5
THD at 500 mW AM: 1 mV input			
30% modulation	%	2.5	5
50% modulation	%	3	6
80% modulation	%	4	8
S/N ratio at 1 mV input	dB	40	35
Image rejection ratio (1st IF/2nd IF)	dB	45	35
1/2 IF rejection ratio (2nd IF)	dB	60	50
IF rejection ratio (1st IF/2nd IF)	dB	70	60
Spurious rejection ratio	dB	50	40
Skirt rejection, 20 kHz single signal	dB	60	50
Cross modulation, RS standard	dB	50	40
Desensitivity at 100 μV desired, 20 kHz away, 3 dB desensitivity	dB	50	40
Oscillator on voltage	V	8.0	10
Current drain at no signal	mA	200	300
Current drain at maximum output	mA	1000	1500
Local emission (Antenna Terminal)	dB m	– 73	– 67

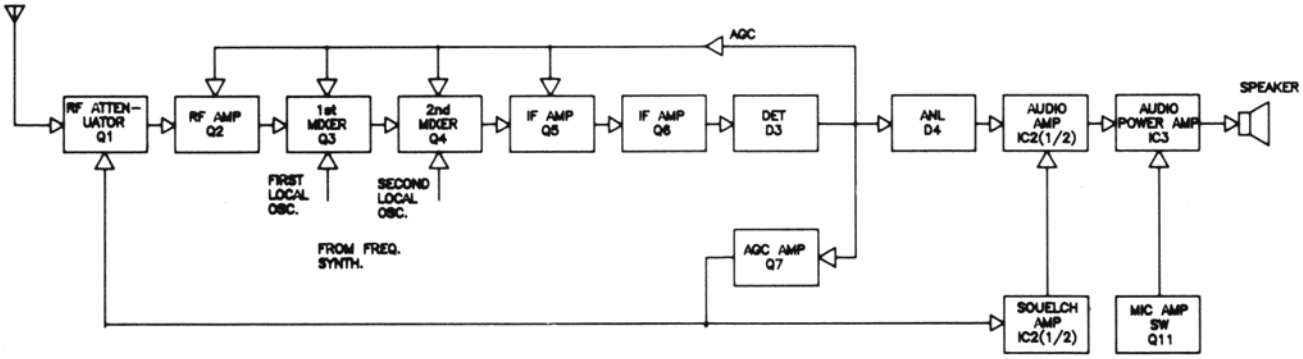
Note: Nominal specs represent the design specs. All units should be able to approximate these – some will exceed and some might drop slightly below these specs. Limit specs represent the absolute worst condition that still might be considered acceptable; in no case should a unit fail to meet limit specs.

BLOCK DIAGRAM

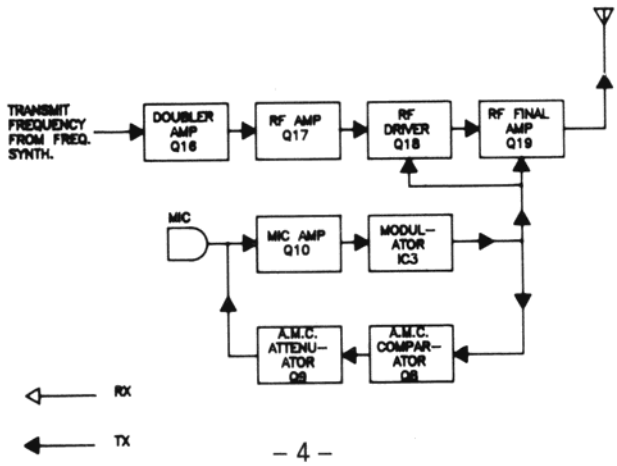
Frequency Synthesizer



Receive



Transmit



CIRCUIT DESCRIPTION

1. General

The TRC–479 is a 40–channel, crystal controlled mobile transceiver which consists of a PLL-synthesizer circuit, a receiver circuit and a transmitter circuit. Diode D12 is a polarity-protector. Power is supplied by a car battery (13.8 V DC). Refer to the Block Diagram and the Schematic Diagram as you read the following descriptions.

2. PLL Synthesizer Section

The TRC–479 uses a Phase-Locked-Loop (PLL) circuit to synthesize the local-oscillator frequencies for receiving and transmitting.

It employs one IC and only one crystal. IC1 is a CMOS large scale integrated circuit containing a reference oscillator, phase detector, active low pass filter, reference divider (1/4096 for transmit, 1/2048 for receive) and a programmable divider.

The programmable divider directly divides the output of the VCO (voltage controlled oscillator) down to a 2.5 kHz (5 kHz for the receiver) signal. Crystal X1 provides a reliable frequency standard which controls the local-oscillator frequencies. The reference-frequency divider inside IC1 counts down the oscillator signal to 1/4096, and passes it on to the phase detector, where it is compared with the 2.5 kHz (5 kHz for receiver) signal from the programmable divider. An error voltage is generated by the phase detector, which is proportional to the phase difference between the two 2.5 kHz (5 kHz for receiver) signals.

This error voltage appears at pin 14 of IC1 and passes through the active LPF (low pass filter), where the error voltage is integrated and harmonics and noise are filtered out. The resulting DC voltage is applied to the varicap diode (D8). Its capacity varies with the applied DC voltage. Because of this capacity change, the output frequency of the VCO is corrected. With proper circuit design and precise adjustments, the VCO frequency is accurate and precise when the system is "locked".

This means that the phase detector senses no phase differences between the two 2.5 kHz (5 kHz for receiver) signals, and the VCO generates a frequency that is as accurate and stable as the reference crystal oscillator. The VCO circuit consists of D8, Q13 and T6.

The circuit is connected in the form of a Hartley oscillator with varicap diode D8 as part of the tank circuit. The VCO circuit generates a signal ranging from 13.4825 to 16.710 MHz. The IC1 also includes an unlock-signal-detector circuit. Should the condition occur, the output at pin 14 of IC1, which is normally open, will be shorted to ground. This means that VCO frequency (1st local oscillator for receiving, 1/2 carrier for transmitting) is "sunk" to pin 14 of IC1 and the transmitter circuit are inhibited.

3. Transmitter Circuit

RF Amplication

The output of doubler amp Q16 is fed through doubler tuning (27 MHz) T7 and T8 to the base of RF amp Q17. The output is then supplied through tuning circuit T9 to RF driver amp Q18. The Q18 output capacitance is devided by tuning circuit L7, C94 and C95 and passed through tuning circuit L8 to the base of final RF stage Q19.

Suppression of Spurious Radiation

The tuning circuit between frequency synthesizer and final amp Q19, and 3 - stage "PI" network C98, L11, C99, L12, C2, L1 and C1 in the Q19 output circuit serve to suppress spurious radiation. This network serves to match Q19 impedance to the antenna and to reduce spurious content to acceptable levels. In-band spurious is reduced to acceptable levels by filtering.

Limiting Power

During factory alignment, the series base resistor of final Q19 (R114) is selected to limit the available power to slightly more than 4 watts. The tuning is adjusted so the actual power is from 3.6 to 3.9 watts, and there are no other controls for adjusting power.

Modulation

The mic input is fed to mic amp Q10 and then to audio power IC3, which feeds the signal to the modulator transformer T5. The audio output at the step up of T5 is fed in series with the B+ voltage through diode D11 to the collectors of Q18 and final Q19 to collector modulate both these stages.

Limiting Modulation

A portion of the modulating voltage is rectified by Q8 to turn on Q9, which attenuates the mic input to mic amp Q10. The resulting feedback loop keeps the modulation from exceeding 100 percent for inputs approximately 40dB greater than required to produce 50 percent modulation. The attack time is about 18 msec. and the release time is about 300 msec.

4. Receiver Circuit

Receiver

The receiver is a double conversion superheterodyne with the first IF at 10.695MHz and the second IF at 455kHz. The synthesizer supplies the first local oscillator 10.695MHz below the received frequency and the second local oscillator at 10.240MHz. The detector output provides reverse AGC to all previous stages except Q6. The AGC voltage is also amplified by Q7 and used to drive RF attenuator Q1, squelch amp and audio amp are IC2.

Indicators

Two additional wafers on the selector switch provide appropriate voltage to a two-digit / seven segment LED display which indicates the selected channel.

When receiving : Q12 base will be high.
Q12 will be turn on.
RX LED indicator (LD202) will light.

When transmitting : D6 cathode will be shorted to ground.
D6 will be turn on.
TX LED indicator (LD203) will light.

FREQUENCIES GENERATED AND MIXED TO OBTAIN EACH CHANNEL

RECEIVE

* VCO FREQUENCY = (N/2048) x REFERENCE FREQUENCY (10.240MHz)

TRANSMIT

* VCO FREQUENCY = (N/4096) x REFERENCE FREQUENCY (10.240MHz)
* TRANSMIT FREQUENCY = VCO FREQUENCY x 2

CHANNEL NUMBER	BCD INPUT TO IC1	RECEIVE		TRANSMIT		
	IC1 PIN NUMBER 8 7 6 5 4 3 2 1	N	VCO FREQUENCY (MHz)	N	VCO FREQUENCY (MHz)	TRANSMIT FREQUENCY (MHz)
1	1 1 1 0 1 1 1 1	3254	16.270	5393	13.4825	26.965
2	1 1 1 0 0 0 0 1	3256	16.280	5395	13.4875	26.975
3	1 1 1 0 1 0 0 1	3258	16.290	5397	13.4925	26.985
4	1 1 1 0 1 0 1 0	3262	16.310	5401	13.5025	27.005
5	1 1 1 1 1 0 0 0	3264	16.320	5403	13.5075	27.015
6	1 1 1 1 0 0 0 0	3266	16.330	5405	13.5125	27.025
7	1 1 1 0 1 1 0 0	3268	16.340	5407	13.5175	27.035
8	1 1 1 0 0 0 0 0	3272	16.360	5411	13.5275	27.055
9	1 1 1 0 1 0 0 0	3274	16.370	5413	13.5325	27.065
10	1 1 0 0 0 1 0 0	3276	16.380	5415	13.5375	27.075
11	1 1 0 0 1 1 1 1	3278	16.390	5417	13.5425	27.085
12	1 1 0 0 0 0 0 1	3282	16.410	5421	13.5525	27.105
13	1 1 0 0 1 0 0 1	3284	16.420	5423	13.5575	27.115
14	1 1 0 0 1 0 1 0	3286	16.430	5425	13.5625	27.125
15	1 1 0 1 1 0 0 0	3288	16.440	5427	13.5675	27.135
16	1 1 0 1 0 0 0 0	3292	16.460	5431	13.5775	27.155
17	1 1 0 0 1 1 0 0	3294	16.470	5433	13.5825	27.165
18	1 1 0 0 0 0 0 0	3296	16.480	5435	13.5875	27.175
19	1 1 0 0 1 0 0 0	3298	16.490	5437	13.5925	27.185
20	0 0 1 0 0 1 0 1	3302	16.510	5441	13.6025	27.205
21	1 0 1 0 0 0 0 1	3304	16.520	5443	13.6075	27.215
22	1 0 1 0 0 0 0 1	3306	16.530	5445	13.6125	27.225
23	1 0 1 0 1 0 0 1	3312	16.560	5451	13.6275	27.255
24	1 0 1 0 1 0 1 0	3308	16.540	5447	13.6175	27.235
25	1 0 1 1 1 0 0 0	3310	16.550	5449	13.6225	27.245
26	1 0 1 1 0 0 0 0	3314	16.570	5453	13.6325	27.265
27	1 0 1 0 1 1 0 0	3316	16.580	5455	13.6375	27.275
28	1 0 1 0 0 0 0 0	3318	16.590	5457	13.6425	27.285
29	1 0 1 0 1 0 0 0	3320	16.600	5459	13.6475	27.295
30	1 0 0 0 0 1 0 0	3322	16.610	5461	13.6525	27.305
31	1 0 0 0 1 1 1 1	3324	16.620	5463	13.6575	27.315
32	1 0 0 0 0 0 0 1	3326	16.630	5465	13.6625	27.325
33	1 0 0 0 1 0 0 1	3328	16.640	5467	13.6675	27.335
34	1 0 0 0 1 0 1 0	3330	16.650	5469	13.6725	27.345
35	1 0 0 1 1 0 0 0	3332	16.660	5471	13.6775	27.355
36	1 0 0 1 0 0 0 0	3334	16.670	5473	13.6825	27.365
37	1 0 0 0 1 1 0 0	3336	16.680	5475	13.6875	27.375
38	1 0 0 0 1 0 0 0	3338	16.690	5477	13.6925	27.385
39	1 0 0 0 1 0 0 0	3340	16.700	5479	13.6975	27.395
40	0 1 0 0 0 1 0 0	3342	16.710	5481	13.7025	27.405

ALIGNMENT PROCEDURES

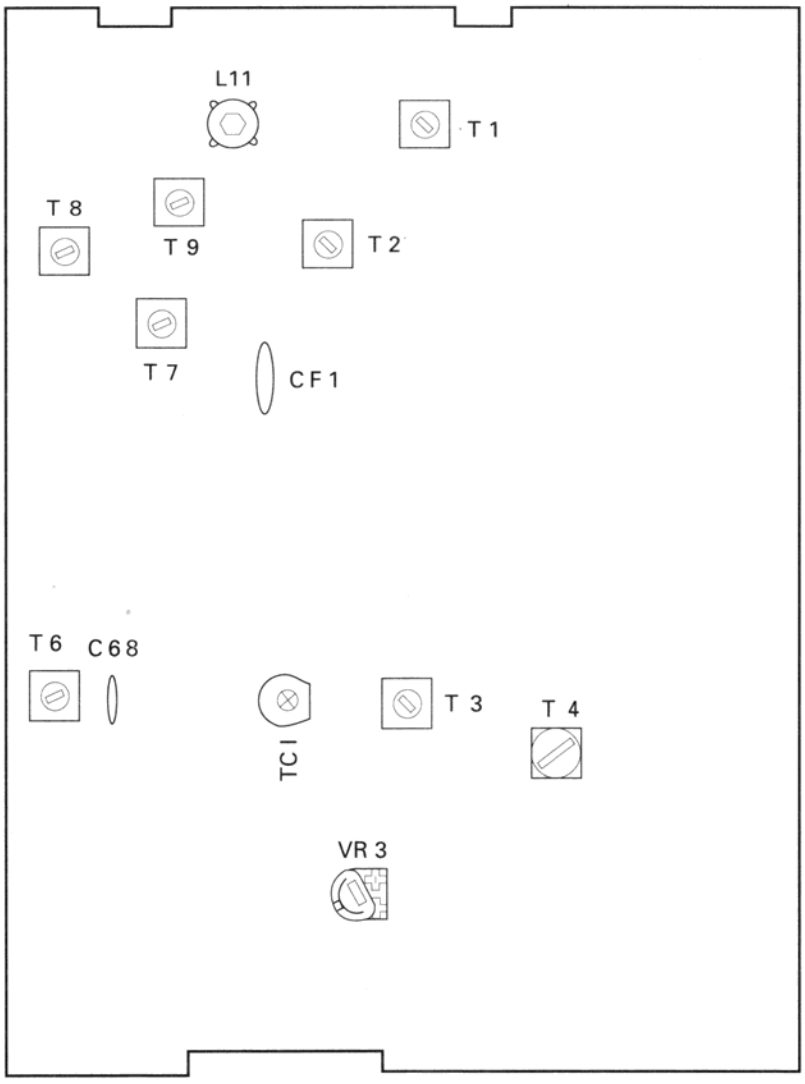


Figure 1

A. PLL SECTION

1. Test Equipment Required

- Frequency counter
- DC voltmeter (above 100 k ohm/V)
- DC power supply (13.8V, 2.5 Amp)

Note: Figure 1 provides test point and all alignment location information.

2. Test Set-up

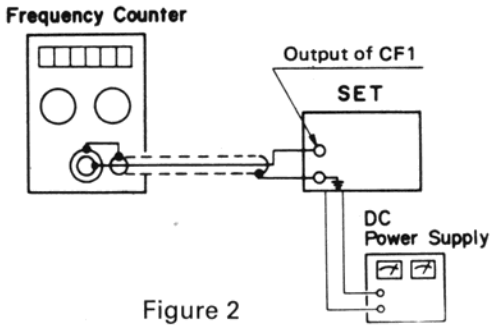


Figure 2

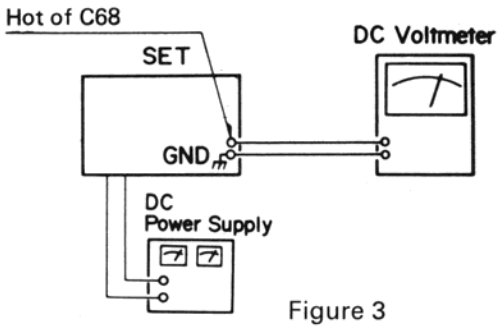


Figure 3

3. Alignment Procedure

STEP	CONTROL SETTING	OUTPUT INDICATOR CONNECTION	ADJUST	ADJUST FOR
1	Alignment of Ref. Osc.			
	MIC: Receive POWER: On VOLUME: Optional SQUELCH: Optional Channel Selector: Channel 19	Connect frequency counter to output of CF1. (Figure 2)	TC1	Adjust for 10.240MHz ±100Hz indication on frequency counter.
2	Alignment of VCO			
	MIC: Transmit POWER: On VOLUME: Optional SQUELCH: Optional Channel Selector: Channel 40	Connect DC voltmeter to hot of C68. (Figure 3)	T6	Adjust for 5.0V indication on DC voltmeter.
3	MIC: Receive POWER: On VOLUME: Optional SQUELCH: Optional Channel Selector: Channel 1	Same as Step 2.	Check the indication on DC voltmeter (must be 2.5–3.5V). If DC voltmeter does not indicate 2.5–3.5V, readjust T6 and reutrn to step 2.	

B. TRANSMITTER SECTION

1. Test Equipment Required

- RF power meter
- 50 ohm load (non-inductive)
- DC power supply (13.8V, 2.5 Amp)
- Field strength meter (or spectrum analyzer with RF attenttator)
- Frequency counter
- Coupler

Note: Figure 1 provides test point and all alignment location information.

2. Test Set-up

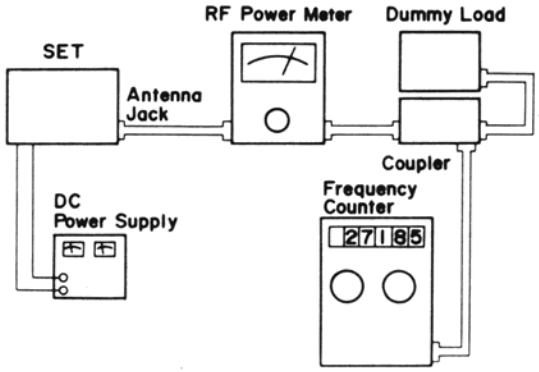


Figure 4

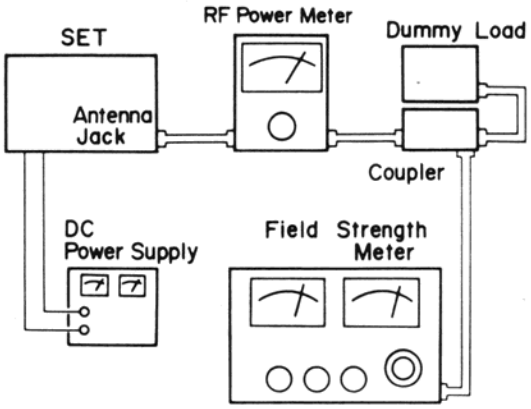


Figure 5

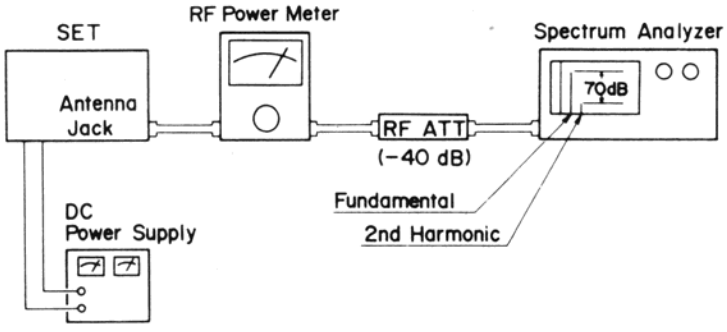


Figure 6

3. Alignment Procedure

STEP	CONTROL SETTING	OUTPUT INDICATOR CONNECTION	ADJUST	ADJUST FOR
1	Alignment of Overall			
	Set channel selector to CH19.	Connect dummy load and frequency counter through coupler to RF power meter. Connect RF power meter to ANT jack on set. (Figure 4)	T7, T8 T9, L11	Adjust for maximum indication on RF power meter.
2	Repeat Step 1 twice or 3 times.			
3	Realignment of T9			
	Set channel selector to CH1.	Same as Step 1.	T9	Adjust for maximum indication on RF power meter.
4	Set channel selector from CH1 to CH19, then from CH19 to CH40.	Same as Step 1.	Check that difference in RF output power between channels is less than 0.2W.	
5	Same as Step 4.	Same as Step 1.	Check that RF output power is 3.8 to 4.2W on all channels with no modulation. If it is not within the above range, go back to steps 1 through 4 and readjust. If still improper, change R114 value.	
6	Alignment of Transmitter Frequency			
	Return to CH19.	Same as Step 1.	TC1	Make sure that the transmitter frequency is 27.185MHz ± 300Hz on frequency counter. If not, readjust TC1.
7	Set channel selector to CH1, CH19, and CH40.	Connect dummy load and field strength meter through coupler to RF power meter. Connect RF power meter to ANT jack on set. (Figure 5) Tune to 2nd harmonic frequency (54.37MHz) on field strength meter. Or connect spectrum analyzer, RF attenuator and RF power meter to ANT jack on set. (Figure 6)	Check level of fundamental and 2nd harmonic frequency (54.37MHz). Check suppression of 2nd harmonic frequency (54.37MHz) compared to fundamental (must be better than 60dB). Check all channels and if necessary, make sure that the 2nd harmonic frequency suppression is more than –60dB on all channels with no modulation. (Reference : –70dB)	

C. RECEIVER SECTION

1. Test Equipment Required

- RF signal generator
- Distortion meter
- SSVM
- Dummy load (8 ohm)
- DC power supply (13.8V, 2.5 Amp)

2. General Alignment Conditions

a. Signal input must be kept as low as possible, to avoid overload and clipping. (Use highest possible sensitivity of output indicator.)

b. Standard modulation is 1000Hz at 30% amplitude.

c. A non-metalic alignment tool must be used for all adjustments.

d. Power supply is adjusted for 13.8V DC, 2A.

Note: Figure 1 shows test point and all alignment location information.

3. Test Set-up

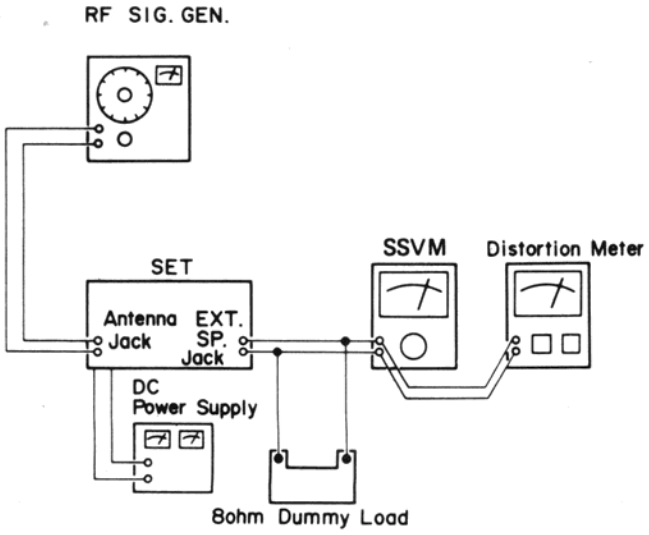


Figure 7

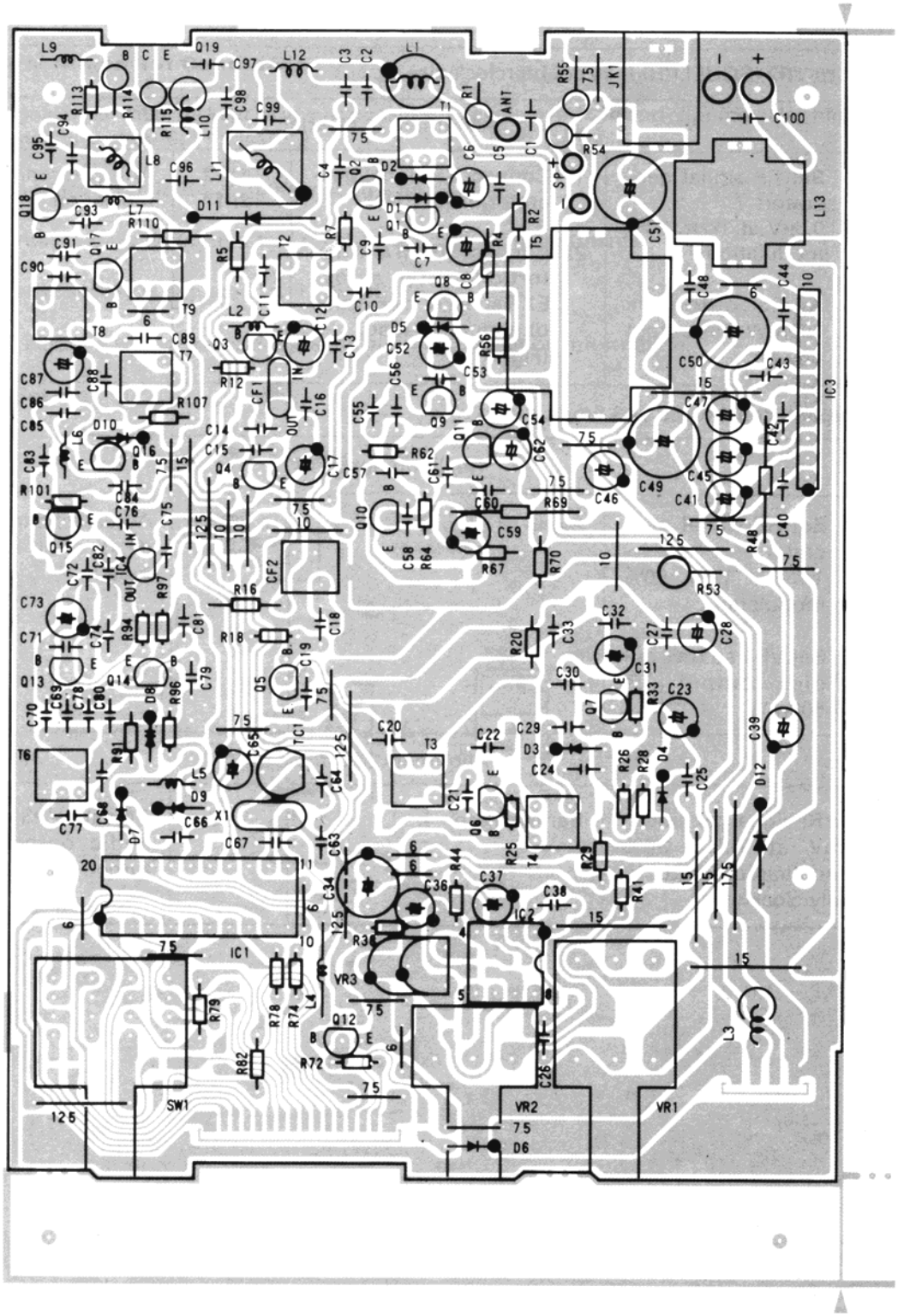
4. Alignment Procedure

STEP	SIGNAL SOURCE CONNECTION	OUTPUT INDICATOR CONNECTION	ADJUST	ADJUST FOR
1	Set channel selector to CH19.			
2	Turn VR1 (VOLUME) fully clockwise.			
3	Turn VR2 (SQUELCH) fully counterclockwise.			
4	Alignment of Overall			
	1) Set RF signal generator: 0.3μV at 1kHz, 30% modulation. 2) Audio output is 500mW (Ref. output power).	1) Connect RF signal generator to ANT jack. 2) Connect SSVM and distortion meter across EXT speaker jack with 8 ohm dummy load. (Figure 7)	T1, T2 T3, T4	Adjust for maximum indication on SSVM.
5	Repeat step 4 twice or 3 times.			
6	Realignment of T4			
	1) Set RF signal generator: 1mV at 1kHz, 80% modulation. 2) Set VR1 so that audio output is 500mW.	Same as Step 4.	T4	Adjust for minimum indication on distortion meter.
7	Alignment of Squelch			
	Set RF signal generator: 1mV at 1kHz, 30% modulation. SQUELCH: Fully clockwise.	Same as Step 4.	VR3	Adjust VR3 so that audio output is just turned on.

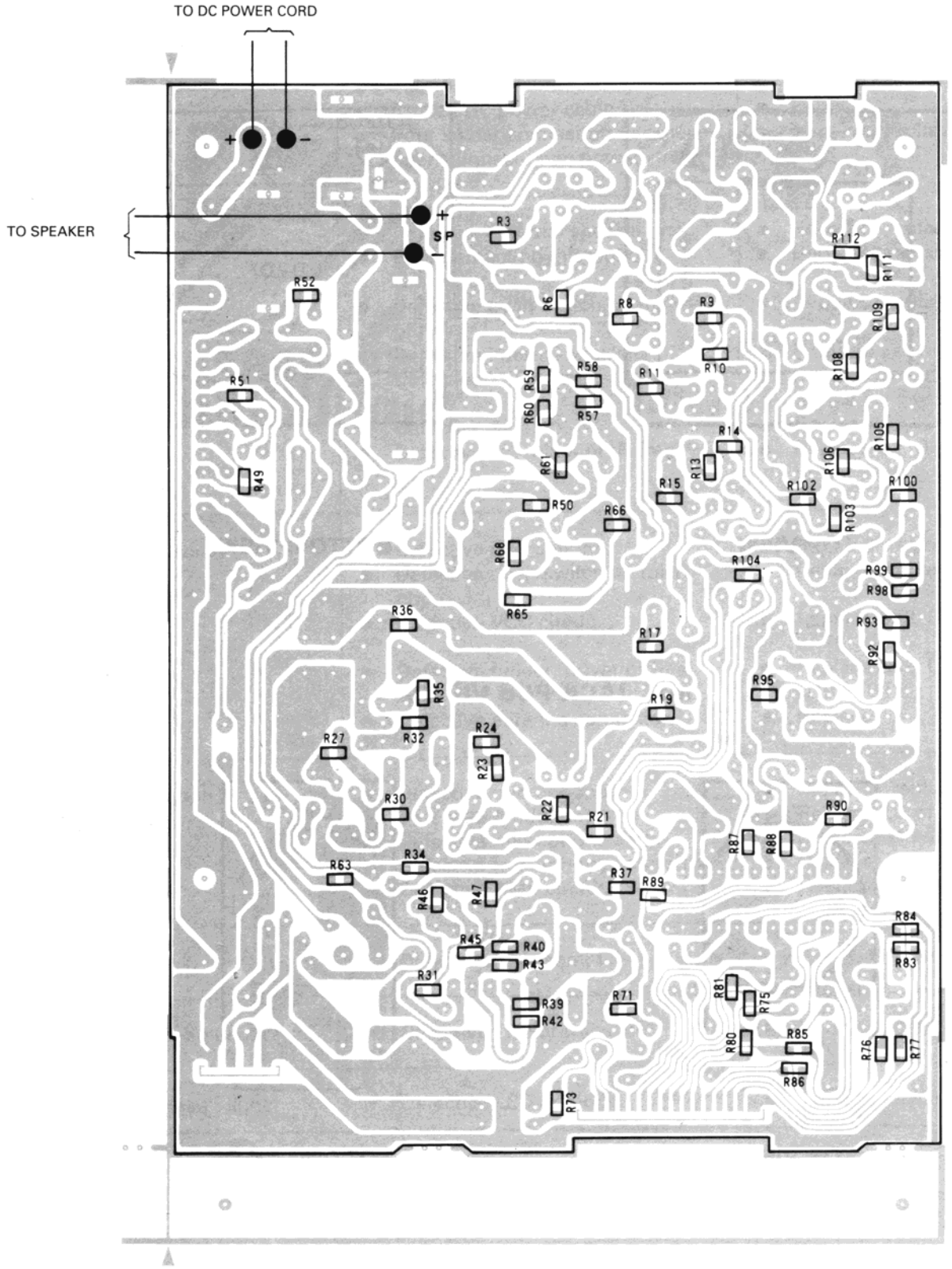
PRINTED CIRCUIT BOARD
(TOP AND BOTTOM VIEW / WIRING DIAGRAM)

MAIN PCB

Top View



Bottom View


TO DC POWER CORD
+
–
TO SPEAKER
+
SP
–
R3
R6
R8
R9
R10
R11
R112
R111
R109
R108
R52
R51
R49
R59
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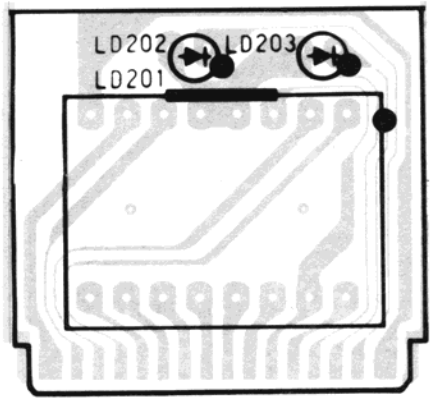
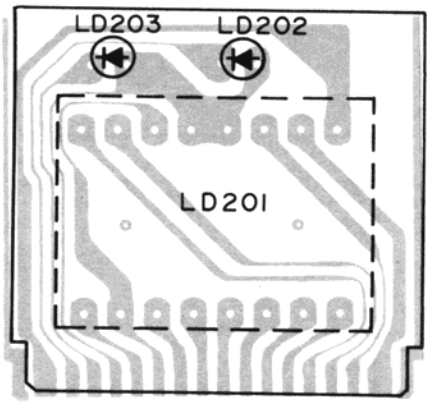
DISPLAY PCB VIEWS

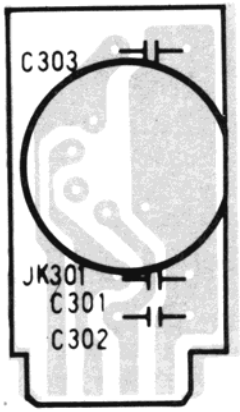


TOP VIEW



BOTTOM VIEW

MIC JACK PCB VIEWS



TOP VIEW

BOTTOM VIEW