

It is possible to utilize the 23 Ch. 02A PLL chassis within the following frequency range: (26.115-27.275MHz).. The only real problem is keeping power up across the entire transmit range to be of use..

The following parts may be changed in most units; (ONLY IF NEEDED); for helping keep the VCO operational at the wider spread of frequencies if needed: C101-increase value no higher than 50pf.; C103 increase value to no higher than 10pf TOTAL. D101 may be changed to a Super Diode also.

Freq. Chart will follow logic states via selector:

1. Pins 9 & 10 isolated, but tied together..
2. Pins 9 & 10 isolated, but tied together. Pin 11-Logic 1.
3. Pin 9 isolated.
4. Pin 9 isolated. Pin 11-Logic 1.
5. Pin 10 isolated.
6. Pin 10 isolated. Pin 11-Logic 1.
7. All normal track (Regular C.B. 23 Ch. F₀).
8. Pin 11-Logic 1

LOGIC 1: Etch feed from selector cut; bridged with a 5.1K 1/4W; apply the PLL logic voltage directly to PLL Pin.

ISOLATED: Pin is completed isolated by cutting the etch feed to the pin or any permanent states which a pin may be tied.

Select.	1	2	3	4	5	6	7	8
1	26.325	26.645	26.965
2	26.335	26.655	26.975
3	26.185	26.345	26.505	26.665	26.825	26.985	27.145
4	26.365	26.685	27.005
5	26.375	26.695	27.015
6	26.385	26.705	27.025
7	26.235	26.395	26.555	26.715	26.875	27.035
8	26.415	26.735	27.055
9	26.425	26.745	27.065
10	26.115	26.275	26.435	26.595	26.755	26.915	27.075	27.235
11	26.125	26.285	26.445	26.605	26.765	26.925	27.085	27.245
12	26.145	26.305	26.465	26.625	26.785	26.945	27.105	27.265
13	26.155	26.315	26.475	26.635	26.795	26.955	27.115	27.275
14	26.165	26.485	26.805	27.125
15	26.175	26.495	26.815	27.135
16	26.195	26.515	26.835	27.155
17	26.205	26.525	26.845	27.165
18	26.215	26.535	26.855	27.175
19	26.225	26.545	26.865	27.185
20	26.245	26.565	26.885	27.205
21	26.255	26.575	26.895	27.215
22	26.265	26.585	26.905	27.225
23	26.295	26.615	26.935	27.255

PATIENCE is the key to building a unit with full coverage.....
 Note: Frequency repeats are not marked on above chart.