



MOTOROLA

MRF463

The RF Line

NPN SILICON RF POWER TRANSISTORS

... designed primarily for applications as a high-power linear amplifier from 2.0 to 30 MHz, in single sideband mobile, marine and base station equipment.

- Specified 28 Volt, 30 MHz Characteristics –
 - Output Power = 80 W (PEP)
 - Minimum Gain = 15 dB
 - Efficiency = 40%
 - Intermodulation Distortion = -32 dB (Max)
- Motorola Improved Single Die Replacement for 2N5942

80 W (PEP) – 30 MHz

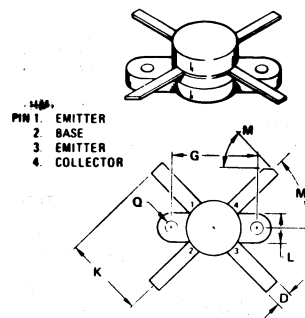
RF POWER TRANSISTOR
NPN SILICON

MAXIMUM RATINGS

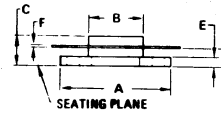
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	35	Vdc
Collector-Base Voltage	V _{CBO}	65	Vdc
Emitter-Base Voltage	V _{EBO}	4.0	Vdc
Collector Current – Continuous	I _C	10	Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	250 1.4	Watts W/°C
Storage Temperature Range	T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.7	°C/W



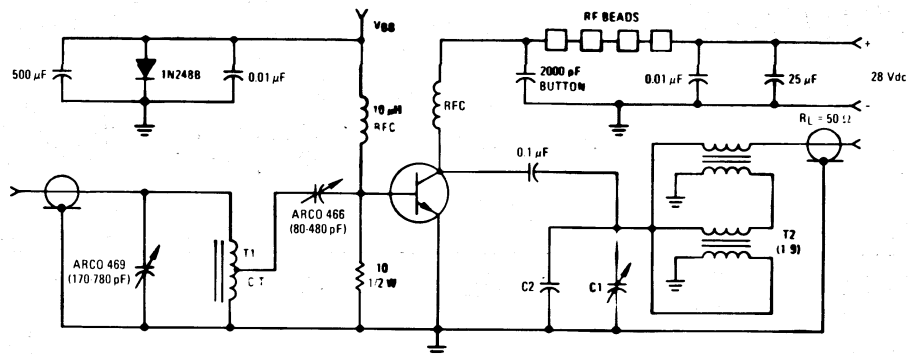
44P
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.64	24.89	0.970	0.980
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	2.15	3.94	0.085	0.155
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	17.78		0.700	
L	6.22	6.48	0.245	0.255
M		45° NOM		45° NOM
N	3.66	4.52	0.144	0.178
O	2.92	3.30	0.115	0.130

CASE 211-10

FIGURE 1—30 MHz TEST CIRCUIT



RF: 20 TURNS #12 AWG ENAMELED WIRE CLOSE WOUND IN 2 LAYERS, 1/4" I.D.
T1: 20 TURNS #24 AWG WIRE WOUND IN MICRO METALS T37-7 TOROID CORE CENTER TAPPED.
T2: 1.9 XFMR, 6 TURNS OF 2 TWISTED PAIRS OF #28 AWG ENAMELED WIRE (8 CRESTS PER INCH) BIFILAR WOUND ON EACH OF 2 SEPARATE BALUN CORES. (Stackpole #57-1503, No. 14 Material reconnected as shown)
RF BEADS: FERROXCUBE #56-590-65 38

V_{BB} adjusted for I_{CQ} 40 mAdc (I_{CQ} = Quiescent Collector Current)

C1 – 170-180 pF ARCO 469 or Equiv.

C2 – 330 pF

MRF463



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 100 \text{ mAdc}, I_B = 0$)	BV_{CEO}	35	—	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 100 \text{ mAdc}, V_{BE} = 0$)	BV_{CES}	65	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 1.0 \text{ mAdc}, I_C = 0$)	BV_{EBO}	4.0	—	Vdc
Collector Cutoff Current ($V_{CE} = 28 \text{ Vdc}, V_{BE} = 0, T_C = +55^\circ\text{C}$)	I_{CES}	—	10	mAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 0.5 \text{ Adc}, V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	10	—	—
DYNAMIC CHARACTERISTICS				
Output Capacitance ($V_{CB} = 28 \text{ Vdc}, I_E = 0, f = 1.0 \text{ MHz}$)	C_{ob}	—	200	pF
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (Figure 1) ($P_{out} = 80 \text{ W (PEP)}, I_C = 3.6 \text{ Adc (Max)}, V_{CC} = 28 \text{ Vdc},$ $f_1 = 30 \text{ MHz}, f_2 = 30.001 \text{ MHz}$)	G_{PE}	15	—	dB
Intermodulation Distortion Ratio (Figure 1) ($P_{out} = 80 \text{ W (PEP)}, I_C = 3.6 \text{ Adc (Max)}, V_{CC} = 28 \text{ Vdc},$ $f_1 = 30 \text{ MHz}, f_2 = 30.001 \text{ MHz}$)	IMD	—	-32	dB
Collector Efficiency ($P_{out} = 80 \text{ W (PEP)}, I_C = 3.6 \text{ Adc (Max)}, V_{CC} = 28 \text{ Vdc},$ $f_1 = 30 \text{ MHz}, f_2 = 30.001 \text{ MHz}$)	η	40	—	%

MATCHING PROCEDURE

In the push-pull circuit configuration two device parameters are critical for optimum circuit performance. These parameters are $V_{BE(on)}$ and h_{FE} . Both parameters can be guaranteed by measuring I_{CQ} of the devices and selecting pairs with a $\Delta I_{CQ} \leq 10 \text{ mAdc}$.

Actual I_{CQ} matching is performed in the MRF463 test circuit with a V_{CE} equal to 28 Volts. The base bias supply is adjusted to set I_{CQ} equal to 40 mAdc using a reference standard MRF463. The I_{CQ} of all production MRF463 transistors is measured using this base bias supply setting. The production MRF463's are tested and categorized in ranges of 10 mAdc. Finally, the devices are stocked as pairs with a guaranteed $\Delta I_{CQ} \leq 10 \text{ mAdc}$.



FIGURE 2 – OUTPUT POWER versus INPUT POWER

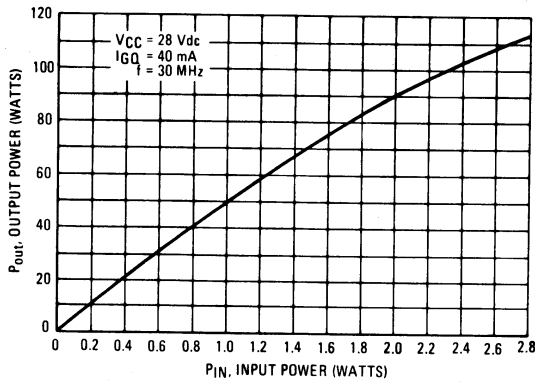


FIGURE 3 – POWER GAIN versus FREQUENCY

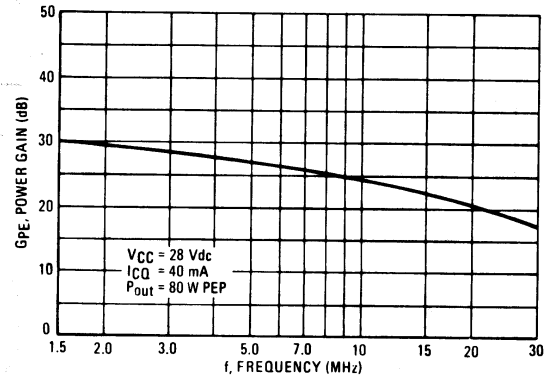


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

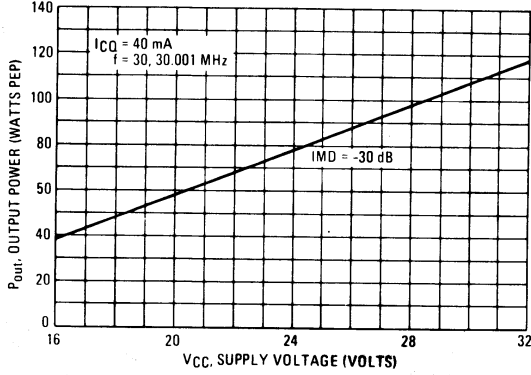


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER

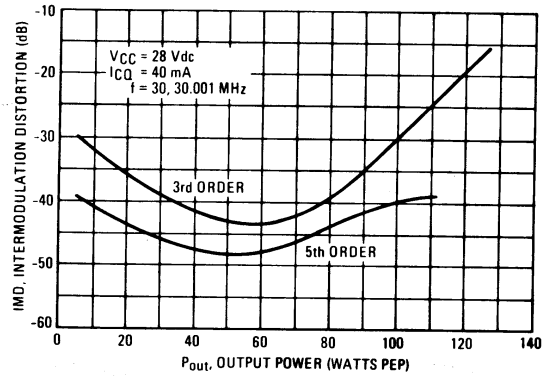


FIGURE 6 – OUTPUT CAPACITANCE versus FREQUENCY

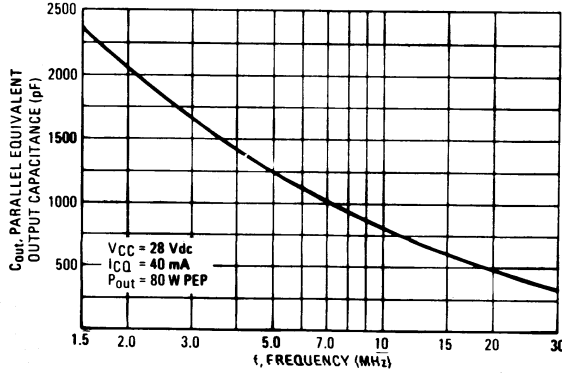


FIGURE 7 – OUTPUT RESISTANCE versus FREQUENCY

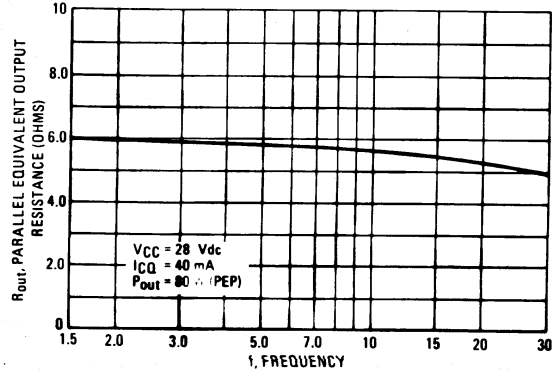




FIGURE 8 - DC SAFE OPERATING AREA

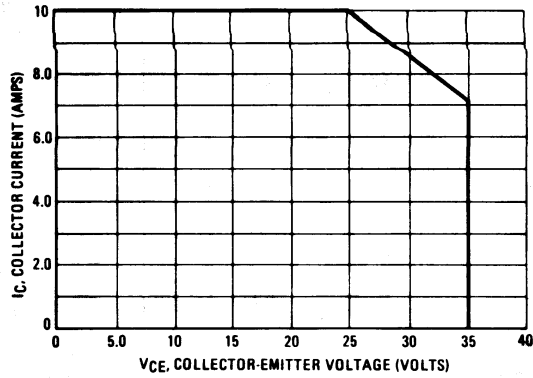


FIGURE 9 - SERIES INPUT IMPEDANCE

